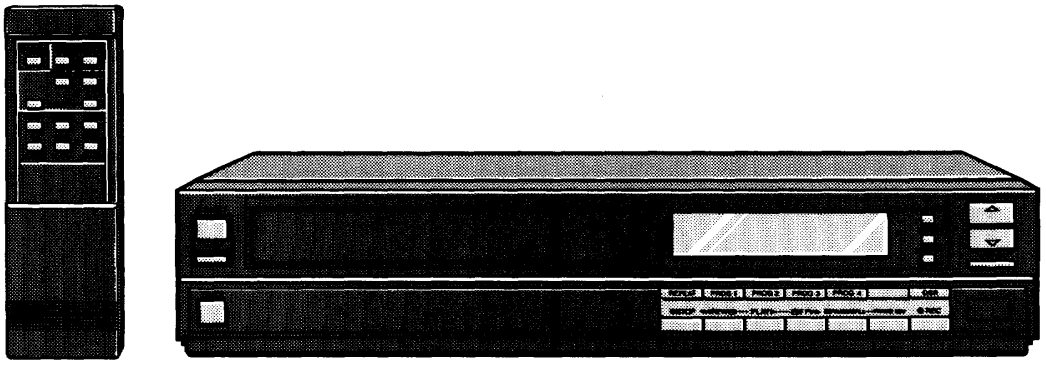
TRAINING MANUAL

SANYO

VHR-3100 Series

Colour Video Cassette Recorder

VHS HQ
PAL



CONTENTS

AP2 SERIES

REFERENCE NO. WM-19746

1. VIDEO CIRCUIT

1-1. OUTLINE

This model employs the same fundamental operating principles as the video circuit described for the conventional VHS system VCR.
Since the video circuit of this model uses the conventional two video head configuration, the video circuit configuration is almost the same as conventional models.
The operation description of the video signal circuit of this model is mainly a explanation of the signal processing ICs.

1-2. VIDEO PRE-AMPLIFIER PROCESSING CIRCUIT

The video pre-amplifier processing circuit is shown in Fig. 1-2-1.

The video signal is obtained from the magnetic tape during playback and is amplified by approximately 60 dB by the pre-amplifier. After the amplified video signal containing the playback Y-FM signal and playback chroma signal receives the necessary signal compensation, it is output to the respective signal processing circuits.
In the record mode, after mixing of the recording Y-signals from the respective signal processing circuits and recording chroma signals, the mixed output is supplied through the rotary head to the video head for recording on the magnetic tape.
The chroma signal the AM component, is recorded on the magnetic tape after overlapping the Y-signal, the FM component, as the AC bias.
Since details of signal processing is exactly the same as signal processing in conventional models, a detailed description will not be repeated here.

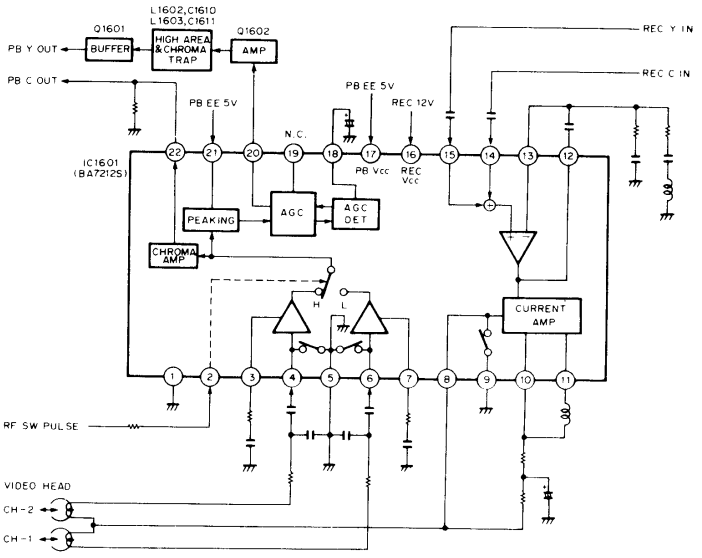


Fig. 1-2-1

[Terminal names of IC1601]

Pin No.	Terminal Name	Pin No.	Terminal Name
1	PB GND	12	REC MIX OUTPUT
2	PB HEAD SWITCH	13	REC 1st FB
3	PRE AC-FB (ch-1)	14	REC CHROMA INPUT
4	PRE AMP CH-1 INPUT	15	REC Y-FM INPUT
5	REC GND	16	REC Vcc
6	PRE AMP CH-2 INPUT	17	PB Vcc
7	PRE AC-FB (ch-2)	18	PB AGC DETECT
8	PRC:OUTPUT, PB:SWITCH IN	19	PB FM OUTPUT
9	PB GND	20	PB FM OUTPUT
10	REC CURRENT DETECT	21	PB PEAKING FILTER
11	REC AC-FB	22	PB CHROMA OUTPUT

Table 1-2-1

1-3. Y-SIGNAL PROCESSING CIRCUIT

The Y-signal system in this model uses a new IC (AN3230K).

Even through the type of IC is different, it still employs the same operating principles for the Y-signal record/playback system that has been described in the conventional VHS models. The difference lies in the IC's internal structure.

Thus, this section will introduce the IC and simply describe circuit operation in the recording/playback modes by the flow of the main signals.

(1) IC1001 (AN3230K)

IC1001 (AN3230K) is an IC for recording/playback of VHS system Y-signals.

This IC integrates the functions of the two ICs of the conventional Y-signal processing system into a single IC. It includes the contemporary high picture quality technology (HQ system) of VHS, or in other words, a detail enhancer.

In addition, through combination with the 1H CCD delay line, playback noise is cancelled by using the correlation between the lines.

Thus, this IC contains all of the fundamental functions for recording/playback with the exception of a head amplifier and recording amplifier. Recording and playback processing of all Y-signals is made possible by combining this IC with the IC (BA7212S) for video signal recording/playback pre-amplification.

Fig. 1-3-1 shows the internal block diagram for IC1001 and peripheral circuit configuration for Y-signal processing.

The IC1001 terminal specifications and IC mode select control are shown in Table 1-3-1 through 1-3-3.

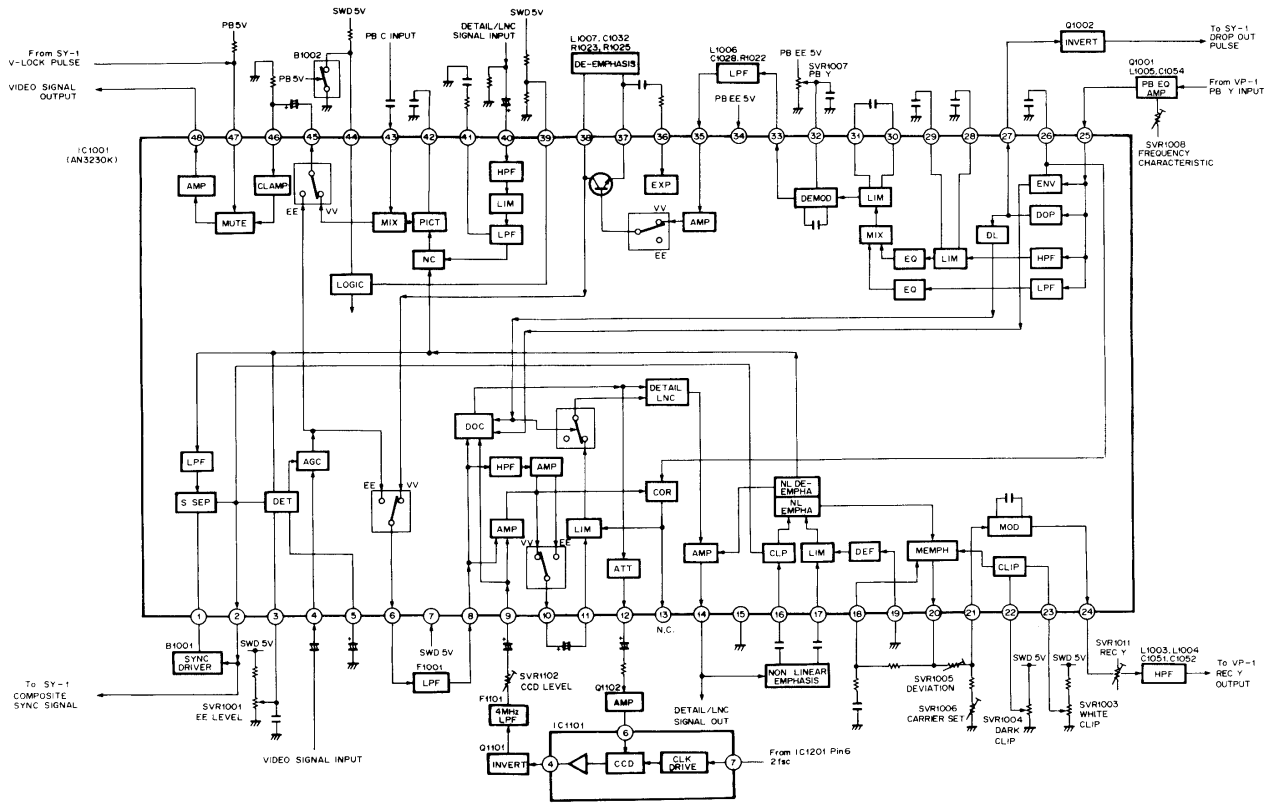


Fig. 1-3-1

[Terminal names of IC1001]

Pin No.	Terminal Name	Pin No.	Terminal Name
1	SYNC TIP LEVEL DETECT	25	PB FM INPUT
2	SYNC SEPARATE PULSE OUT	26	ENVELOPE DETECTION
3	EE LEVEL ADJ.	27	DROP OUT PULSE OUT
4	EE:VIDEO SIGNAL INPUT	28	DOUBLE LIMITER HPF SIDE BIAS (1)
5	AGC DETECTION	29	DOUBLE LIMITER HPF SIDE BIAS (2)
6	AGC/MAIN DE-EMPHASIS OUT	30	MAIN LIMITER BIAS (1)
7	Vcc	31	MAIN LIMITER BIAS (2)
8	DETAIL/LINE NOISE CANCEL MAIN SIGNAL IN	32	FM DEMODULATOR GAIN CONTROL
9	LINE NC (1HDL) SIGNAL IN	33	FM DEMODULATOR OUT
10	HIGH PASS LIMITER OUT/DIFFERENCE DETECT OUT	34	EXC. REC Vcc
11	LINE NC LIMITER IN	35	PB VIDEO SIGNAL INPUT
12	1HDL CCD OUT	36	VIDEO EXPANDER
13	CORRELATION DETECT OUT	37	VIDEO PEAKING
14	DETAIL/LINE NC OUT	38	MAIN DE-EMPHASIS
15	GND	39	EDIT MODE SELECT
16	MAIN CLAMP IN	40	NC LIMITER IN
17	NON LINEAR LIMITER IN	41	NC LPF
18	FEED BACK AMP IN	42	PICTURE CONTROL
19	PG PULSE IN & 2H/4, 6H	43	PB CHROMA IN
20	MAIN EMPHASIS OUT	44	HQ:EE/VV SELECT
21	FM MODULATOR IN	45	EE/VV OUTPUT
22	DARK CLIP LEVEL ADJ.	46	SOFT CLAMP IN
23	WHITE CLIP LEVEL ADJ.	47	DUMMY SYNC PULSE IN
24	FM MODULATOR OUT	48	VIDEO SIGNAL OUTPUT

Table 1-3-1

[IC1001 mode select level]

Pin No.	Level	Voltage Control (V)	Mode Condition
44	H	3.8 ~ 5.0	HQ, EE
	M	1.6 ~ 2.9	EE
	L	0 ~ 0.7	VV
39	H	3.8 ~ 5.0	EDIT
	M	1.6 ~ 2.9	NORMAL
	L	0 ~ 0.7	
47	H	3.8 ~ 5.0	SYNC-TIP
	M	1.6 ~ 2.9	GRAY
	L	0 ~ 0.7	THROUGH
19	H	2.3 ~ 3.3	4H, 6H High
	M	1.7 ~ 1.9	4H, 6H Low
	L	0 ~ 0.9	2H

Table 1-3-2

[IC1001 mode select control table]

Level		Mode Condition	EE		Correlation Detect Pulse	VV			
			Detail Enhancer			LNC		NC	Picture Control
Pin 44	Pin 39		SP	LP		SP	LP		
H	M	EE (A)	ON	OFF	ON *1	—	—	—	—
	H	EE, EDIT	OFF	OFF	ON *1	—	—	—	—
L	M	VV (B)	—	—	ON	OFF	ON	ON	ON
	H	VV, EDIT	—	—	ON	OFF	ON	*2	OFF
M	M	EE	OFF	OFF	ON *1	—	—	—	—
	H	EE, EDIT	OFF	OFF	ON *1	—	—	—	—
L	M	VV	—	—	ON	OFF	ON	ON	ON
	H	VV, EDIT	—	—	ON	OFF	ON	*2	OFF
M	L	EE	ON	OFF	ON *1	—	—	—	—
	H	EE, EDIT	OFF	OFF	ON *1	—	—	—	—
L	L	VV	—	—	ON	ON	ON	ON	ON
	H	VV, EDIT	—	—	ON	OFF	ON	*2	OFF
M	L	EE	OFF	OFF	ON *1	—	—	—	—
	H	EE, EDIT	OFF	OFF	ON *1	—	—	—	—
L	L	VV	—	—	ON	ON	ON	ON	ON
	H	VV, EDIT	—	—	ON	OFF	ON	*2	OFF

(Notes)

*1: When line correlation detection is made during recording, the DC potential of pin-26 is forced to the high level.

*2: In the VV EDIT mode, the peak values for the amount of NC noise cancellation are approximately 6 dB less than normal.

*3: The EDIT mode is not used in this model.

Table 1-3-3

(2) RECORDING

The input video signal is routed from the LINE input terminal or tuner unit to IC1001 pin-4. The video signal input to pin-4 of IC1001 passes through the AGC amplifier and is split to EE monitor and recording video signals.

In the AGC circuit, the signal from sync separation and the sync tip clamped signal from IC1001 pin-16 are adjusted to a set level and the mixed signal passes through AGC detection where the amplitude of the video signal is fixed.

The EE monitor is output from pin-45 of IC1001 and is routed to pin-46 for clamping where it is set to the tip level of the sync signal. It then passes through the mute circuit and amplifier and is output as the line output from pin-48 and to the RF converter.

The recording video signal is output from pin-6 of IC1001 and passes through the F1001 low-pass filter. This removes unnecessary chroma signal components and extracts the REC Y-signal.

The REC Y-signal is input to IC1001 pin-8 and the main signal is output to the detail enhancer from DOC. The minute mid and high frequency signal components of the sub-signal are extracted by the high pass filter, amplifier, and limiter and output to the detail enhancer. The detail enhancer strengthens the minute signal levels of the high-range portion of the Y-signal frequency characteristics.

As shown in recording mode Table 1-3-3 (A), detail/LNC operates as a detail enhancer by the control provided by pin-44 and pin-39 of IC1001.

The REC Y-signal which passed through the detail enhancer passes through the amplifier and is output from IC1001 pin-14. Then, before frequency modulation, it is necessary to enhance the high-range of the signal to reduce the effects of noise, and at the same time the S/N ratio is improved. Pre-emphasis is made using the non-linear emphasis characteristics. This operation is performed by the non-linear emphasis circuit and main emphasis circuit, and it enhances the mid and high-range characteristics of the Y-signal. Non-linear emphasis is by the non-linear characteristics circuit configured by resistors, capacitors, and limiters. Then, this signal is combined with the clamped signal input from pin-16 of IC1001, and the Y-signal is frequency modulated after adjustment of dark clipping and white clipping by the main emphasis circuit.

The amount of deviation and sync tip carrier for frequency modulation are adjusted in the FM modulation circuit and the REC Y-FM signal is output from IC1001 pin-24.

After adjustment of the recording current of the REC Y-FM signal, the interference with the recording signal of the low-range conversion chroma sub-carrier (627 kHz) is eliminated by the HPF (trap filter).

This signal is then output to the VP-1 board as the REC Y-signal.

(3) PLAYBACK

The playback Y-FM signal is separated from the playback video signal picked up from the video head by the video pre-amplifier circuit on the VP-1 board.

The playback Y-FM signal is input to IC1001 pin-25 after adjustment of its frequency characteristics to the vicinity of approximately 5 MHz by the playback equalizer amplifier.

The playback Y-FM signal input to IC1001 pin-25 is output to the dropout detection and envelope detection circuits.

The dropout pulses output from pin-27 are used by the noise cancellation circuit of the servo circuit and also pass through an internal delay circuit for compensation of the noise occurring during dropout correction and signal switching. As dropouts occur constantly at regular intervals during special playback, etc., it is necessary to stop the dropout compensation operation. This is performed by envelope detection, and this output is output to the dropout compensation circuit and is also output to the noise cancellation circuit which uses line correlation. The dropout compensation circuit can be thought of as a kind of switch, and it eliminates the long dropouts (noise bars) of the envelope detection output during special playback.

The playback Y-FM signal input to IC1001 pin-25 is split into signals which pass through the low-pass and high-pass filters.

The signal which passed through the high-pass filter passes through a limiter and is combined with the signal which passed through the low-pass filter. This enhances the upper waveband of the playback Y-FM signal.

The mixed signal is output to the FM demodulation circuit after amplitude limitation by the limiter again. This circuit operates in the same manner as the conventional double limited circuit. The FM demodulation circuit uses the conventional FM demodulation system (consisting of limiter, FM detector, and integrator) to restore the playback Y FM signal to the original Y-signal and also to adjust the level of the Y-signal.

The playback Y-signal which passed through the FM demodulation circuit is output from IC1001 pin-33 and the frequency component which is double the carrier (occurs during demodulation) is removed by the low-pass filter.

This signal is then input from pin-35, passes through the amplifier, and is output to the de-emphasis circuit for playback.

The de-emphasis circuit can be thought of as the reverse of pre-emphasis for recording. The high-range of the signal is attenuated to return it to its original characteristics and the noise components which occur during frequency conversion are attenuated to improve the S/N ratio.

The playback Y-signal with its original characteristics restored by the de-emphasis circuit is output from

IC1001 pin-6, and the noise components in the vicinity of 8 MHz are removed after FM demodulation by the low-pass filter. Next, the playback Y-signal is input to IC1001 pin-8 and the main signal is output to detail/LNC from the dropout compensation circuit.
The detail/LNC operates as an LNC (line noise canceller) according to control from pins 44 and 39 of IC1001, as shown in Table 1-3-3 (B) for playback.
When there is a dropout during playback, the main signal output from pin-12 passes through the 1H CCD delay line and 4 MHz LPF, is output to the dropout compensation circuit from Pin-9, and is input to the LNC from the DOC to form a closed loop. This performs dropout compensation.
When there is no dropout, the main signal is simply input to the LNC from the DOC.
The 1H delay line uses the conventional glass delay line to create a 1H delay when there is a dropout in the FM Y-signal.
This model uses a CCD (charge coupled device) to allow the demodulated Y-signal to be delayed with no change.
Since the base band of the Y-signal can also be delayed, the dropout compensation range is made wider as the noise which occurs when the signal is restored is greatly reduced.
The effectiveness of cancellation for comb noise is especially increased.
In terms of performance, the CCD operation can be effectively controlled from the low range to the bandwidth set by the sampling frequency, rather than the wide bandwidth of conventional glass delay lines.
In principle, the sampling frequency for the 1H CCD is fsc (color sub-carrier). However, playback is only possible up to a bandwidth of one-half the sampling frequency. If this limit is exceeded, the spectra will overlap and returning noise will occur.
Thus, a sampling frequency which is at least twice the required bandwidth is used.
Since IC1201 of the chroma signal processing system of this model is equipped with a 2 f_{SC} output terminal, this signal is used as the sampling frequency.
The 4 MHz low-pass filter removes the returning noise components.
The following explanation deals with the noise cancellation circuit which uses the line correlation.
Video signals uses a correlation of approximately 1H, and signals without correlation are assumed to be noise. This noise components is eliminated by adding a reverse phase signal to the video signal. As Y-signal of approximately 1H have strong correlation, a signal difference of approximately 1H will mean that only the noise components lacking line correlation will be obtained. This noise canceller only works properly when there is high vertical correlation, in other words when the two continuous scan lines have the same signal.
Thus, noise cancellation using line correlation functions in the same manner as comb filter for minute signals, eliminating cross-talk of line correlation and preventing a drop in resolution when there is no line correlation.
In this model, the main signal is input from IC1001 pin-8 and is output from the DOC switch to the LNC.
The noise components of sub-signal are output to the LNC after passing through high-pass filter, amplifier, pins 10 and 11, and the limiter.
In the LNC, the noise components are cancelled by subtracting the sub-signal from the main signal (original signal).
Also, the main signal input from IC1001 pin-8 and the 1H DL signal input from pin-9 are supplied to the respective amplifier circuits and the differential noise component is extracted.
This signal is input to the line correlation detection circuit together with the envelope detection output.
Output from the limited is then prevented by applying the line correlation detection signal to the limiter.
In other words, when there is no line correlation, the signal and noise components are output from the limiter, but when there is line correlation, only the noise components are output to the LNC.
The playback Y-signal which passed through the line noise canceller, passes through the amplifier and is output from IC1001 pin-14. It is clamped by the reverse characteristics of the non-linear characteristics for recording and passes through the non-linear de-emphasis circuit. This signal is then output to the noise canceller which uses a high-pass filter.
The playback Y-signal output from IC1001 pin-14 is also input to pin-40, and the signal which passes through the high-pass filter, limiter, and low-pass filter is output to the noise canceller.
The high-range portion of the Y-signal is extracted by the high-pass filter, and after the limiter removes the noise components of the small signal levels, the low-pass filter reduces the signal to the bandwidth for which the noise canceller is effective. This noise canceller regards the low-level signals in the high-range portion of the Y-signals as noise and cancels the noise by subtracting this from the original signal.
After the picture quality is set by the picture control, the signal is combined with the playback chroma signal (PBC) and the playback video signal is output from IC1001 pin-45.
The playback video signal is input to clamping from IC1001 pin-46, aligned with the tip level of the sync signal and is output to the mute circuit.
V-LOCK pulses (dummy vertical sync signal) are input to the mute circuit from the servo circuit to prevent wavering of vertical synchronization during special playback.
The playback video signal passes through the amplifier after the mute circuit, is line output from IC1001 pin-48 and is output to the RF converter.

1-4. CHROMA SIGNAL PROCESSING CIRCUIT

This model uses a new IC (TA8632N) for the chroma signal system. Even through the type of IC is different, it still employs the same operating principles for the chroma signal record/playback system that has been described in the conventional VHS models. The difference lies in the IC's internal structure.

Since this model uses a 1 H CCD delay line with IC for the 1 H delay of the Y-signal, 2 • f_{SC} (4.433619 MHz) is output from pin-6 of the IC1201 for driving the clock of this IC.

Thus, this section will introduce the IC and simply describe circuit operation in the recording/playback modes by describing the flow of the main signals.

(1) IC1201 (TA8632N)

IC1201 (TA8632N) is a playback/recording IC for VHS system chroma signals.

Compared to the IC (TA8604N) used for conventional chroma signal processing systems, there are the following changes in the internal operation of the IC.

- When there is chroma signal output from pin-30, the color killer operation during recording is OFF. This is because it is used for the SECAM detection operation circuit.
- Gate pulses are no longer to the APC detection filter at pin-7. This is to improve f_{SC} deviation in the SECAM mode for models equipped for both PAL and SECAM systems.

In the same manner as the conventional IC (TA8604N), this IC contains all of the basic recording/playback functions for the chroma signal processing system, and this single chip performs all chroma signal recording/playback processing for the various TV broadcast systems (NTSC, PAL, and SECAM).

The internal block diagram of IC1201 is shown in Fig. 1-4-1 as well as the peripheral circuit configuration for chroma signal processing. The terminal specifications of IC1201 and IC mode select control tables are shown in Tables 1-4-1 through 1-4-2.

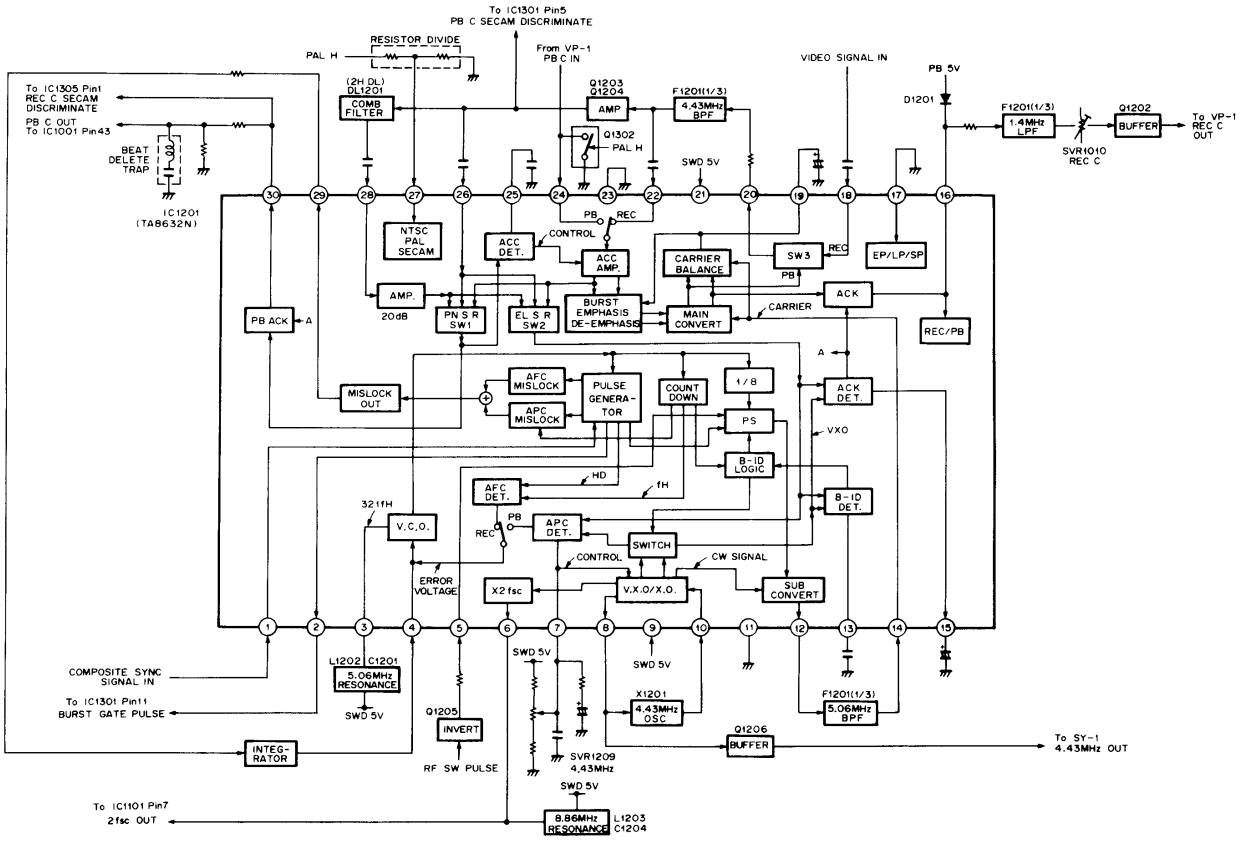


Fig. 1-4-1

[IC1201 terminal characteristics]

Terminal		Standard DC voltage	Input/output impedance	Standard AC voltage	Remarks	Terminal		Standard DC voltage	Input/output impedance	Standard AC voltage	Remarks
No.	Name					No.	Name				
1	Composite sync signal input	———	40 kΩ	High 4.7V Low 0V	Sync: positive pulse VCO reference signal	16	REC: chrome out PB: select in	2.4V (ACK: 0V) 4.0V or higher: PB mode	30 Ω	Burst signal 600m Vp-p	Sink current: 1.0 mA
2	Burst gate pulse output	———	Open omitter	High 4.3V Low 1.3V	Sync: negative pulse	17	EP/LP/SP select input	EP: 5V LP: 2.5V SP: 0V	50 kΩ or higher (open base)	———	Controls SW1 burst emphasis
3	V.C.O. time constant	———	10 kΩ	430 mVp-p	Collector output	18	REC video signal input	2.5V	20 kΩ	Composite video signal 1Vp-p	Differentiation input
4	V.C.O. control filter	2.4V	10 kΩ when gate; other: current drive	———	With clamp (HIGH 3.4V) (LOW 1.6V)	19	DC feedback filter	2.9V	Current drive	———	For ACC amp., main convert, DC balance adj.
5	Color rotary pulse input	———	40 kΩ	High 4.7V Low 0V	CH1: High CH2: Low	20	B.P.F. drive output	2.3V	SEPP	Burst signal 300 mVp-p	REC: Chroma + ΔY PB: 4.21MHz ± 629kHz
6	X2 Isc output	———	4 kΩ	0.6 Vp-p	Collector output	21	Vcc 2	(5.0V)	———	———	ACC, Main convert, Chrome output system
7	V.X.O. control filter	2.4V	10 kΩ when gate; other: current drive	———	With clamp (HIGH 3.4V) (LOW 1.6V)	22	REC chrome signal input	2.7V	20 kΩ	Burst signal 150 mVp-p	———
8	V.X.O. output	———	30 Ω	1.2 Vp-p	Sink current: 1.0mA	23	GND 2	———	———	———	ACC, Main convert, Chrome output system
9	Vcc 1	(5.0V)	———	———	For VCO, VXO, sub convert, B-ID, logic	24	P8 chroma signal input	2.7V	20 kΩ	Burst signal 150 mVp-p	———
10	V.X.O. input	3.1V	———	0.3 Vp-p	———	25	ACC filter	———	Current drive	———	With clamp (HIGH 3.8V) (LOW 2.2V)
11	GND 1	———	———	———	For VCO, VXO, sub convert, B-ID, logic	26	Chroma signal input 1	2.4V	10 kΩ	Burst signal 300 mVp-p	———
12	Sub converter output	4.4V	1 kΩ	1.2Vp-p	Collector output	27	NTSC/PAL/ SECAM select input	NTSC: 5.0V SECAM: 2.5V PAL: 0V	50 kΩ or higher (open base)	———	———
13	Burst-ID filter	3.0V	5 kΩ	1.6 Vp-p	———	28	Chroma signal input 2	2.7V	20 kΩ	Burst signal 38 mVp-p	———
14	Conversion carrier input	2.7V	1 kΩ	240 mVp-p	———	29	Mislock filter	———	Current drive	———	———
15	ACK filter	2.2V	10 kΩ when gate; other; current drive	———	HIGH: ACK OFF LOW: ACK ON	30	Chroma signal output	2.7V (PB ACK: 0V)	30 Ω	Burst signal 300 mVp-p	Sink current: 1.0mA

Note: Characteristics of terminals may vary depending on the Vcc voltage used and other conditions.
The characteristics in the above table are standard values at Vcc = 5V and Tn = 25°C.

Table 1-4-1

[IC1201 mode select control table]

Mode select Note 2			Mode status			
V_{16}	V_{27}	V_{17}				
H	H	H	NTSC playback mode • 320 f_H VCO is controlled by APC loop.	SW1 is connected to output side of comb filter (pin-28)	SW2 : connected to output side of comb filter (pin-28)	With burst de-emphasis
		M				No burst de-emphasis
		L			SW2 : connected to input side of comb filter (pin-26)	With burst de-emphasis
	M	H	SECAM playback mode • APC loop only	SW1 is connected to input side of comb filter (pin-26)	Status of SW2 is not important in SECAM mode	No burst de-emphasis
		M				
		L				
	L	H	PAL playback mode • 321 f_H is controlled by APC loop. • The reference signal to B-ID and APC loop is reversed every 1H.	SW1 is connected to output side of comb filter (pin-28)	SW2 : connected to output side of comb filter (pin-28)	
		M				
		L			SW2 : connected to input side of comb filter (pin-26)	
L (open) Note 1	H	H	NTSC recording mode • Controlled by AFC, APC loop system	SW1 and SW2 are connected to ACC amplifier side		With burst de-emphasis
		M				No burst de-emphasis
		L				With burst de-emphasis
	M	H	SECAM recording mode • AFC loop only			No burst de-emphasis
		M				
		L				
	L	H	PAL recording mode • Controlled by AFC, APC loop system • The reference signal to B-ID and APC loop is reversed every 1H.			
		M				
		L				

Note 1: Also low-range conversion chroma output terminal for recording.
Note 2: V_{16}, V_{27}, and V_{17} indicate the voltage levels of IC1201 pin-16, pin-27, and pin-17 respectively.
Note 3: The voltage levels of V_{27} and V_{17} are as follows:
H level : 5V
M level : 2V
L level : 0V
Note 4: The NTSC mode is not used in this model.

Table 1-4-2

(2) RECORDING

The input video signal is input from either the LINE input terminal or tuner to IC1201 pin-18. The video signal input to IC1201 pin-18 and after passing through switch 3 is output from pin-20 to the 4.43 MHz band-pass filter.

The 4.43 MHz band-pass filter passes 4.43 MHz band chroma signal, and the signal is input to the ACC amplifier after passing through the REC/playback switch from pin-22 of IC1201.

The ACC amplifier amplifies the chroma signal so that its amplitude is at a set level. Then, the chroma signal is output to the main converter to down-convert into 627 MHz after 6 dB emphasize of the burst level by the burst emphasis circuit.

A carrier signal of approximately 5.06 MHz (4.43 MHz + (40 f_H + 1/8 f_H)) is input to the main converter from IC1201 pin-14.

The main converter is used to balance-modulate the 4.43 MHz chroma signal in order to down-convert the recording chroma signal to 626.953 kHz.

The down-converted chroma signal output from the main converter is supplied to the ACK (automatic color killer) circuit and then output to IC1201 pin-16. After down-converted chroma signal passes through the 1.4 MHz low-pass filter to remove the higher band signals, the recording level is adjusted and the signal is output to the VP-1 board as the REC C (record chroma) signal.

(3) PLAYBACK

The playback video signal output from the VP-1 board goes into IC1201 pin-24, goes through the REC/playback select switch and is input to the ACC amplifier. The ACC amplifier amplifies the playback chroma signal with keeping chroma burst signal in constant level.

Then, the playback chroma signal is input to the main converter to re-convert into 4.43 MHz original frequency after 6 dB attenuation of the burst level by the burst de-emphasis circuit.

In the same manner to the record mode, a carrier signal of approximately 5.06 MHz (4.43 MHz + (40 f_H + 1/8 f_H)) is input to the main converter, where the playback chroma signal is converted to 4.43 MHz by means of the balanced modulation.

The frequency converted chroma signal is output through switch 3 from IC1201 pin-20. The chroma signal is passed through the 4.43 MHz band-pass filter to remove the unwanted frequency components, amplified and routed to a comb filter which removes the color cross-talk signal (the luminance signal component that is included in the chroma signal band width). The chroma signal is again input from IC1201 pin-28, routed through the amplifier, switch 1, ACK, and then output from pin-30 to the Y/C mix circuit of the luminance signal system IC.

1-5. SECAM DISCRIMINATION CIRCUIT

The SECAM discrimination circuit is shown in Fig. 1-5-1.

The SECAM discrimination circuit is for areas in which PAL system and pseudo-SECAM (ME-SECAM) system television broadcasts can be received.

For countries which have only PAL system television broadcasts (such as the UK) and countries which have true SECAM (SECAM L) broadcasts (such as France), refer to the circuit diagrams and operational descriptions of models capable of receiving these television broadcasts.

The 1-5. SECAM Discrimination Circuit is omitted from VCR models for areas in which only PAL system television broadcasts are made, and this section is unnecessary.

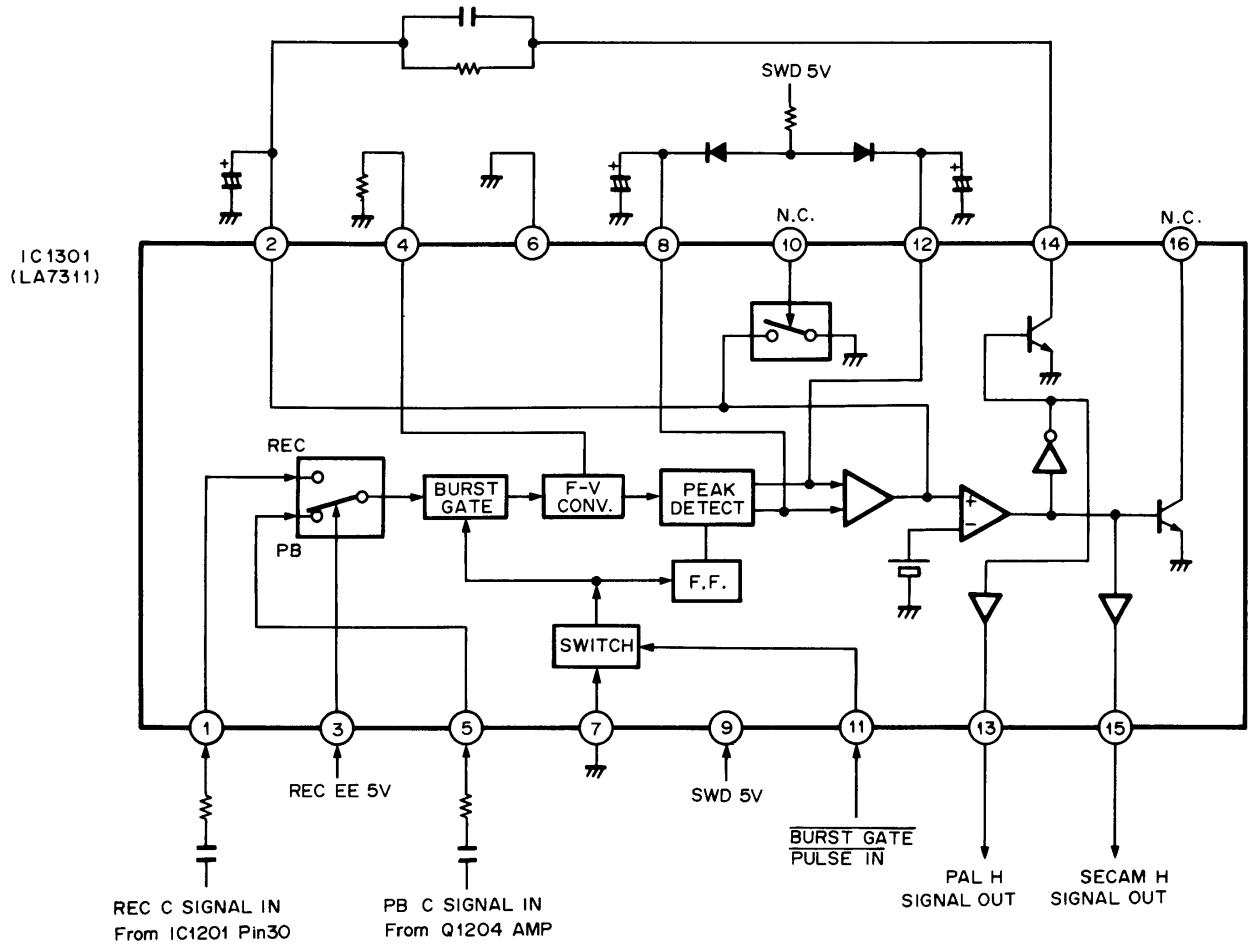


Fig. 1-5-1

Pin No.	Terminal Name	Pin No.	Terminal Name
1	REC CHROMA INPUT	9	Vcc
2	SECAM HOLDER	10	PAL HIGH IN
3	REC/PB CONTROL IN	11	$\overline{\text{BGP}}$ IN
4	CURRENT SOURCE	12	PEAK FILTER (2)
5	PB CHROMA INPUT	13	PAL HIGH OUT
6	GND	14	PAL DRIVE
7	BGP IN	15	SECAM HIGH OUT
8	PEAK FILTER (1)	16	SECAM DRIVE

Table 1-5-1

The main portion of circuit operations of the SECAM discrimination circuit are made by the new IC (LA7311) used in this model.
Operational block diagrams of the IC are shown in Fig. 1-5-2 and 1-5-3, and the following is an explanation of this circuit.
The SECAM discrimination circuit extracts the burst signal (or H-ID signal) from the chroma signal and detects whether there is a difference every 1H (1 horizontal synchronization period.) This determines whether the signal is SECAM system (4.25 MHz or 4.41 MHz) or PAL system (4.43 MHz) and outputs a signal to the chroma signal processing IC (TA8632N) to select the proper mode for this IC.

[Description of each block]

• SWITCH

This switches the pin-3 REC/playback control voltage between chroma signal input (pin-1) for recording and chroma signal input (pin-5) for playback.

• BURST GATE CIRCUIT

The burst signal (or H-ID signal) is extracted from the chroma signal according to the burst gate pulse input from pin-7 or pin-11.

• F-V CONVERTER

Voltage corresponding to the frequency of the input signal is output.

• FLIP-FLOP

The burst gate pulse is divide and normal and reversed square waves are output.

• INTERMITTENT LEVEL SHIFT

According to the output of the flip-flop, the output DC level of the F-V converter is shifted down every 1H. Thus, the two intermittent level shift circuits alternately shift the level every 1H.

• PEAK DETECTOR

This circuits holds the peak value of the output waveform from the intermittent level shift circuits.

• DIFFERENTIAL AMPLIFIER

The differential DC voltage output from the peak detector is amplified.
With the output voltage at PAL signal input as Vo, the output voltage for SECAM signal input is Vo + α.

• COMPARATOR 1

This compares the output from the differential amplifier and reference voltage E1 (approx. Vo + 1/2α).

• C3

This capacitor holds the output voltage (pin-2) of comparator 1.
The level is low (0V) for PAL signal input and high (approx. 4.2V) for SECAM signal input.

• COMPARATOR 2

This compares the voltage at pin-2 and reference voltage E2 (approx. 1.9V).
When $V_2 < 1.9V$, the output is low level → PAL
When $V_2 > 1.9V$, the output is high level → SECAM

• COMPULSION PAL

This circuit forces the PAL signal input state from pin-10.

• DRIVER

When the comparator 2 output is low, 20 mA of current flows to pin-14 of the PAL drive. When the comparator 2 output is high, 20 mA of current flows to pin-16 of the SECAM drive.

• DISCRIMINATION

When the comparator 2 output is low, pin-13 is driven high by the PAL discrimination circuit. When the level is high, pin-15 is driven high by the SECAM discrimination circuit.

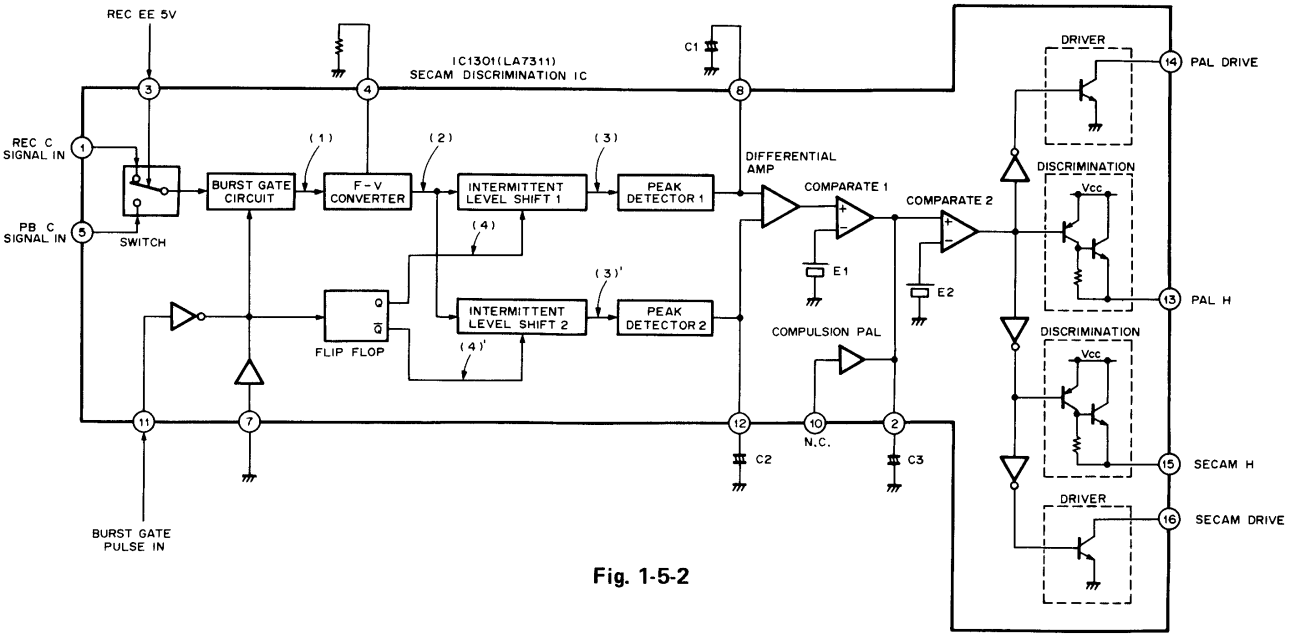


Fig. 1-5-2

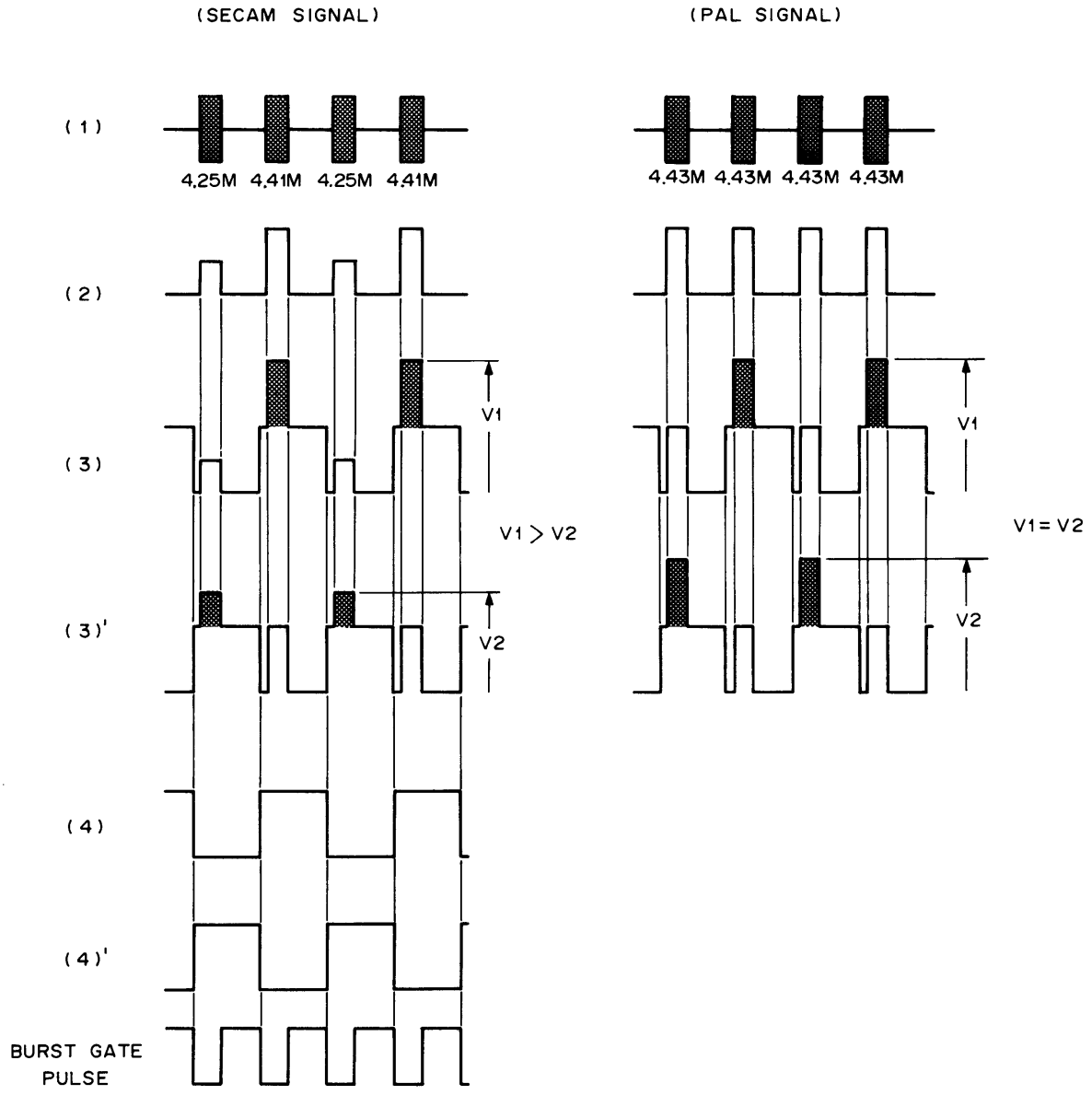

(SECAM SIGNAL)
(PAL SIGNAL)
(1)
4.25M 4.41M 4.25M 4.41M
4.43M 4.43M 4.43M 4.43M
(2)
(3)
(3)'
(4)
(4)'
BURST GATE PULSE
V1
V2
V1 > V2
V1
V2
V1 = V2

Fig. 1-5-3

2. AUDIO CIRCUIT

2-1. OUTLINE

The audio circuit is composed mainly of audio signal record/playback use exclusive IC (LA7096) and ac bias oscillator circuit.

IC2001 (LA7096) is exclusive IC for audio signal record and playback of VCR, that has built-in necessary functions for audio signal processing within a single chip requiring a small number of peripheral components.

Bias oscillator circuit provides ac bias current to audio R/P head during record mode while it supplies erase current to full erase head and to audio erase head at the same time.

Operating functions of the IC (LA7096), IC2001's pin terminals and the record/playback modes will be described as follows.

(1) Record/playback amplifier
- Equalizer amplifier
- Line amplifier
- Recording amplifier

(2) ALC (Automatic Level Control) and detector circuit
(3) Ripple filter (two stage configuration)
(4) Muting control circuit
(5) REC/EE, and PB/EE respective select switches
(6) Playback muting and record muting output circuits

[Terminal names of IC2001]

Pin No.	Terminal Name	Pin No.	Terminal Name
1	HEAD SELECT SWITCH IN	16	AUDIO LINE OUTPUT
2	RIPPLE FILTER	17	ALC FILTER
3	RIPPLE FILTER	18	REC SIGNAL INPUT
4	EP SWITCH IN	19	LP SWITCH IN
5	HEAD SELECT SWITCH IN	20	EP SWITCH IN
6	PB AUDIO SIGNAL INPUT	21	REC AMP NFB
7	LP SWITCH IN	22	REC AUDIO SIGNAL OUTPUT
8	EP SWITCH IN	23	LP CONTROL SIGNAL IN
9	EQUALIZE AMP NFB	24	EP CONTROL SIGNAL IN
10	GND	25	MUTE CONTROL SIGNAL IN
11	EQUALIZE AMP OUTPUT	26	PB/EE CONTROL SIGNAL IN
12	PB SIGNAL OUTPUT	27	V_{CC}
13	AUDIO LINE INPUT	28	OSCILLATOR BIAS
14	LINE AMP NFB	29	REC/EE CONTROL SIGNAL IN
15	GND	30	REC/PB EE SWITCH COMMON

Table 2-1

2-2. RECORD MODE

Audio input signal is introduced from VD-1 board to IC2001 pin 13 during record mode. The audio input signal amplitude is automatically controlled by ALC circuit that is built-in IC2001, and is then fed to the record/playback select switch.

The ALC circuit functions to control the input signal amplitude automatically when the input signal amplitude exceeds a pre-set level that is determined by ALC detection circuit. It controls gain of line amplifier so that audio signal will not be recorded exceeding tape's saturation level. The ALC detection circuit uses line amplifier's output signal as its reference signal that is converted into dc signal and is then fed back to the ALC circuit. The ALC circuit's attack time and recovery time is determined by the time constant circuit which is connected to IC2001 pin 17.

The REC-EE/PB select switch detects the PB 5V signal that is input to IC2001 pin 26, with the PB/EE control circuit. The detected output drives the IC2001 internal switch to either REC-EE position so that the audio signal is supplied to the line amplifier.

The line amplifier output audio signal is amplified by about 35 dB and is then supplied from pin 16 to the VD-1 board as the REC EE monitor signal.

The line amplifier output from pin 16 is also supplied to the record level control circuit, is passed through record muting circuit from IC2001 pin 18 and is then supplied to record amplifier. The record amplifier provides frequency equalization too.

The audio signal output from IC2001 pin 22 is added to ac bias signal that is supplied from 70 kHz oscillator circuit, and is supplied to audio R/P head to be recorded on magnetic tape.

2-3. PLAY MODE

Playback signal that is picked up by audio R/P head from magnetic tape is input to IC2001 pin 6 and is routed to the IC's internal equalization amplifier. The equalization amplifier has built-in playback equalizer circuit that provides de-emphasis during playback mode in contrary to the pre-emphasis (frequency response correction to suit for magnetic recording characteristics) during recording.

The playback audio signal that has now flat frequency response characteristics by the equalization amplifier, after being adjusted its playback level, is routed from IC2001 pin 12 to PB muting circuit.

The PB/EE select circuit inside IC is switched to PB position by the PB 5V of IC2001 pin 26 during playback mode.

The playback audio signal from line amplifier is output to the VD-1 board same as the EE monitor signal in the record mode.

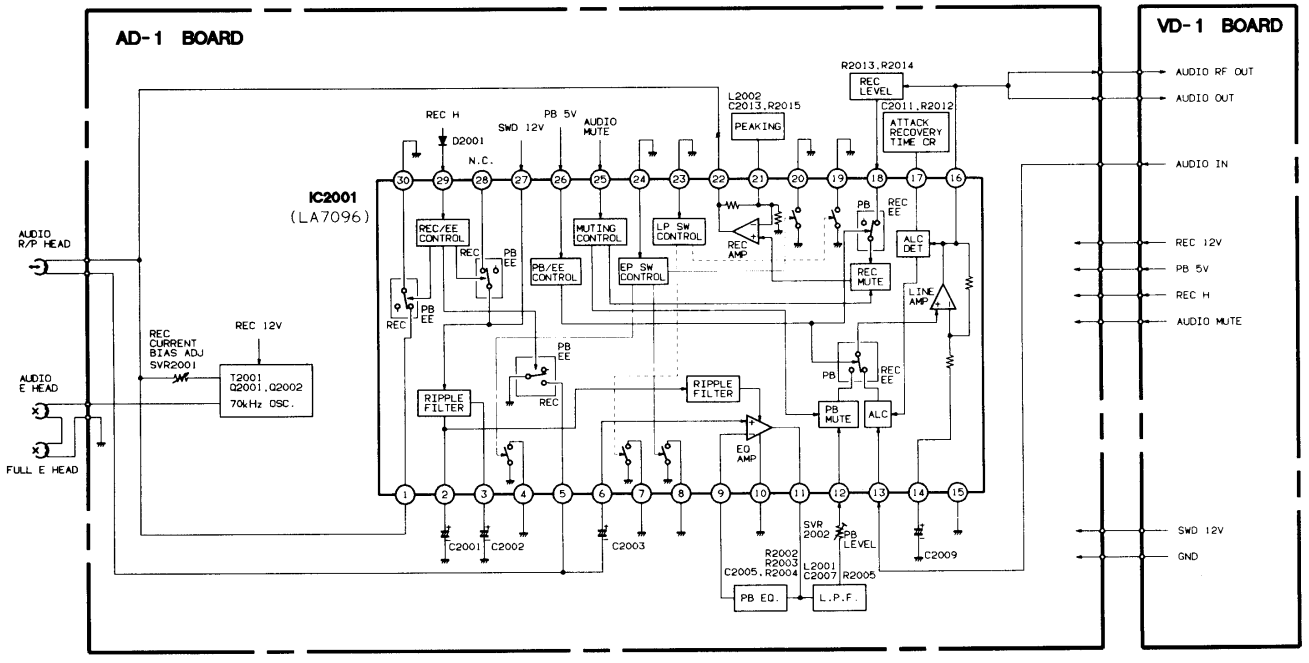


Fig. 2-1

3. SERVO CIRCUIT

3-1. SERVO CIRCUIT OUTLINE

Outline of servo control circuit, head motor rotation and capstan motor rotation are shown in Fig. 3-1 block diagram. The servo control circuit consists mainly by two ICs where one is a digital servo IC that has a built-in data ROM for control data, and the other is IC that amplifies the servo control signal.

The servo control circuit has two functions of speed control and phase control. Output of these two control signals are mixed so that the servo motor drive voltages are generated. The servo control system provides a stable record and playback pictures. The speed servo control system receives FG signal from motor so that the rotating data of the motor is input to IC where FG frequency is compared with the internally memorized pre-set frequency data inside ROM of the digital IC. The comparison output is the error voltage output for speed servo control system.

The phase servo control system compares reference signal's phase with that of PG signal, FG signal or playback CTL signal that are the motor rotating data. The comparison outputs are time difference between the reference phase and motor rotation. The compared time difference output is again compared with the pre-set time difference data that is already memorized internally inside ROM of the digital IC. The comparison output is the error voltage output for phase servo control system.

The speed servo error output and the phase servo error output are mixed by a differential amplifier and are supplied to motor drive amplifier circuits as the servo motor drive voltages.

SERVO CIRCUIT PRINCIPLE BLOCK DIAGRAM

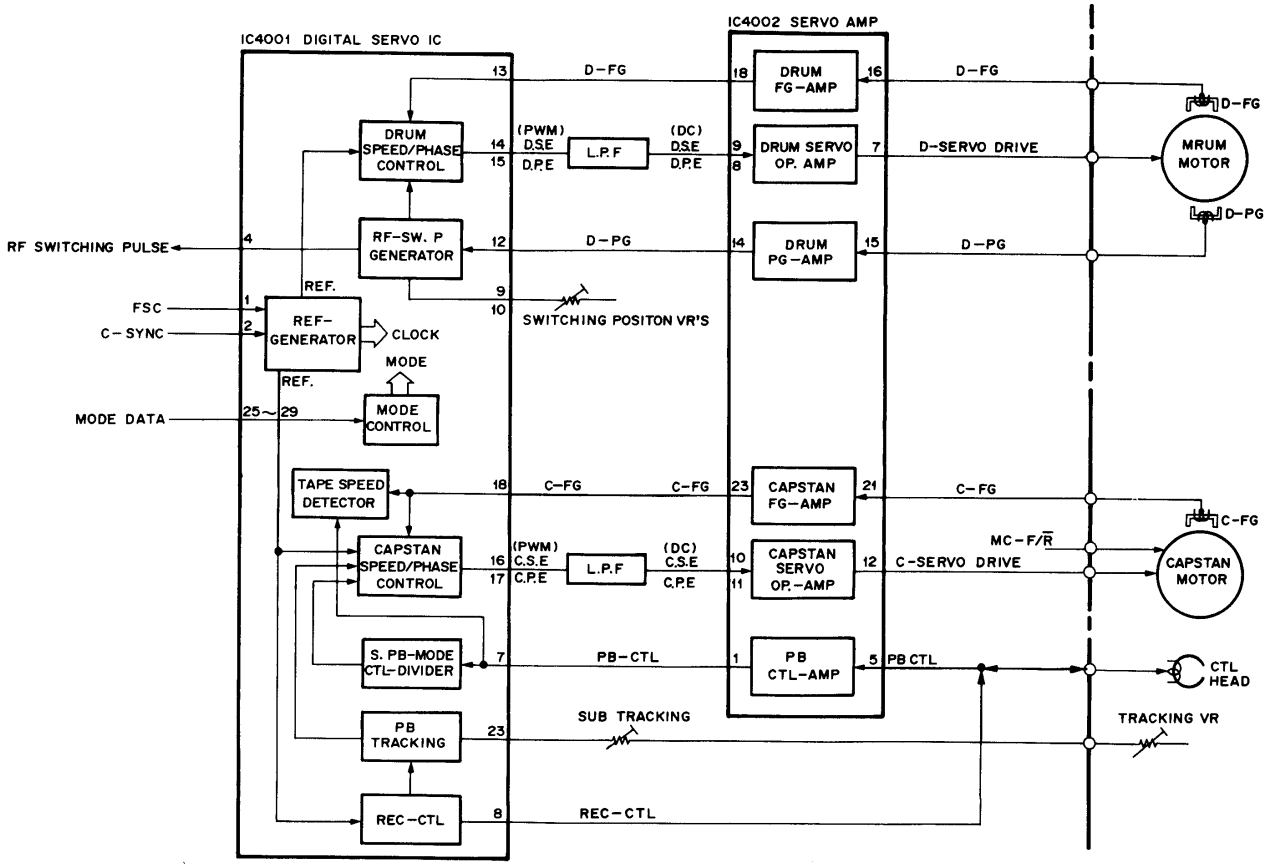


Fig. 3-1

3-2. DIGITAL SERVO IC, IC4001 (LC7412 series/Fig. 3-2)

This IC is CMOS-LSI designed for digital servo control systems. This IC has built-in ROM (read only memory) inside that is able to provide various servo control characteristics data if the ROM's address is specified from external servo mode informations. This IC has the following functions internally.

Digital servo IC internal functions

- Drum servo system: speed servo control/phase servo control (built-in ROM).
- Capstan servo system: speed servo control/phase servo control (built-in ROM).
- Internal reference signal generator to be used for phase control servo (built-in ROM).
- Mode control with control input of 4 bit parallel data.
- Control (CTL) signal record and playback switching.
- Playback mode's tape speed automatic detection (SP/LP/EP).
- Frequency division function for incoming data such as control (CTL) signal and capstan FG signal during special playback mode.
- Drum PG signal processing.
- Dummy VD (V-LOCK) pulse generation during special playback mode.
- Switching signal generation to be used for Hi-Fi head.

IC4001 INTERNAL BLOCK DIAGRAM

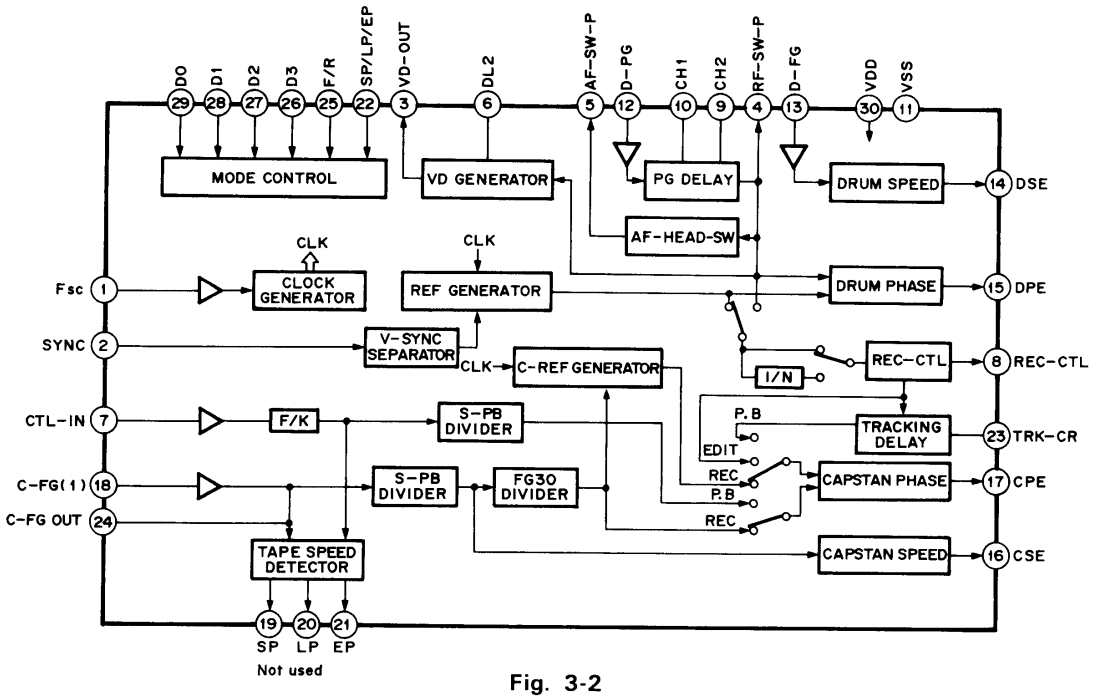


Fig. 3-2

The major internal functions of the IC are described as follows.

(1) MODE CONTROL (Fig. 3-3, Table 3-1)

This IC receives VCR's respective operating mode information (STOP, REW/F.FWD, PLAY, REC, F/R SEARCH etc.,) from system control circuit in the form of 4 bit parallel data. The 4 bit parallel data are used as address data to locate respective data (such as drum speed servo system, drum phase servo system, capstan speed servo system, capstan phase servo system, REF signal generator circuit, special playback frequency division circuit) in accordance with the current operating mode of VCR, in order to select proper servo control system, as shown in Fig. 3-3.

When the current operating mode is detected, input signal selection for use of the reference signal and comparing signal in the capstan phase servo system, is also made.

IC4001 MODE CONTROL BLOCK

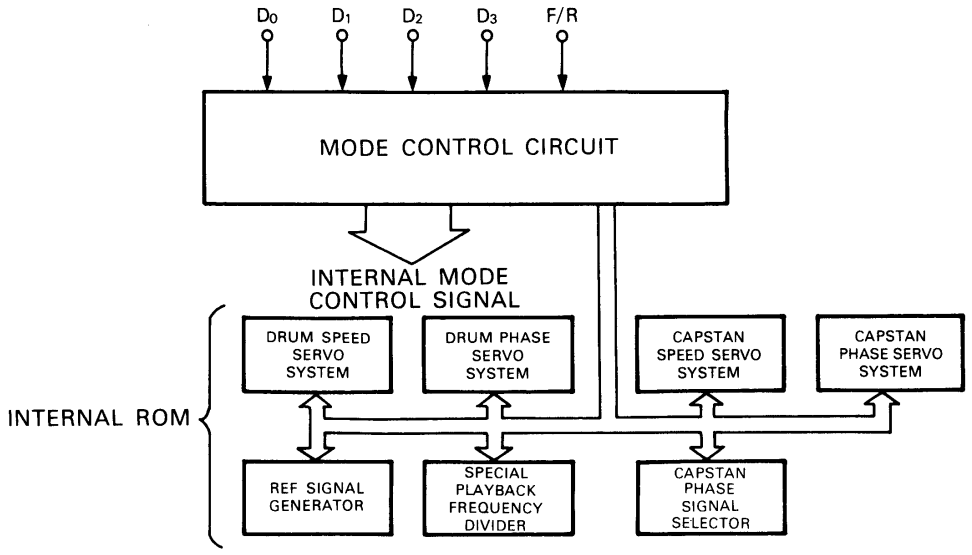


Fig. 3-3

MAJOR MODES OF DIGITAL SERVO IC

HEX. CODE	4-BIT MODE DATA IN				OPERATING	OPERATING CONDITIONS OF DIGITAL SERVO IC			
	D3	D2	D1	D0		DRUM SPEED CONT.	DRUM PHASE CONT.	CAPSTAN SPEED CONT.	CAPSTAN PHASE CONT.
0	0	0	0	0	STOP	LOW OUTPUT	50% DUTY PWM FIXED	LOW LEVEL	50% DUTY PWM FIXED
1	0	0	0	1	FRONT LOADING	LOW OUTPUT	50% DUTY PWM FIXED	P.B.×6 SPEED PWM CONT.	50% DUTY PWM FIXED
2	0	0	1	0	TAPE LOADING	PWM CONT.	50% DUTY PWM FIXED	LOW LEVEL	50% DUTY PWM FIXED
3	0	0	1	1	F.FWD+FEW	LOW OUTPUT	50% DUTY PWM FIXED	P.B.×7 SPEED PWM CONT.	50% DUTY PWM FIXED
7	0	1	1	1	RECORD	PWM CONT.	PWM CONT.	PWM CONT.	PWM CONT.
8	1	0	0	0	EDIT	PWM CONT.	PWM CONT.	PWM CONT.	PWM CONT.
A	1	0	1	0	NORMAL PLAYBACK	PWM CONT.	PWM CONT.	PWM CONT.	PWM CONT.
C	1	1	0	0	SEARCH×5 (P.B.)	PWM CONT.	50% DUTY PWM FIXED	PWM CONT.	PWM CONT.
E	1	1	1	0	STILL	PWM CONT.	PWM CONT.	LOW LEVEL	50% DUTY PWM FIXED

Table 3-1.

(2) DRUM SERVO'S/CAPSTAN SERVO'S PHASE CONTROL LOOP REFERENCE SIGNAL GENERATION. (Fig. 3-4.)

(a) Drum servo's reference signal generator

Record mode

The drum servo's phase control loop selects the vertical sync signal that is separated from the input recording video signal, during record mode.

This IC generates the reference signal as follows : the color subcarrier signal (fsc) is divided to generate the clock signal which is reset by the separated vertical sync using internal REF counter circuit. This method of generating the reference signal, as shown in Fig. 3-5, is free from noise interference into sync signal period or from loss of sync signal, helping to realize stable servo operation.

If a recording without incoming sync (such as audio only recording in Hi-Fi recording) is going to be made, the servo reference signal is generated from the internally built-in ROM data by driving counter circuit. The reference signal thus generated is not only used in the drum servo phase control circuit but also supplied to the CTL-REC circuit and is recorded on magnetic tape control (CTL) track to be used as the capstan phase comparing signal during playback mode. The REC-CTL circuit is made by digital one shot multivibrator with built-in ROM. The ROM provides data of delay time (value corresponds to tape speed) that compensates for the physical length (x value in Fig.3-5) between video head and control signal, and also provides data to determine duty cycle of the REC-CTL signal. See Fig. 3-5.

Playback mode

In playback mode, the reference signal is internally generated by the built-in ROM that provides data to the REF counter which resets the clock signal generated from the color subcarrier (fsc) signal,to make ref. signal. During the picture search playback, the different ROM data are provided to change the frequency of reference signal to compensate for the change of fH frequency. Thus the stable drum phase control servo is maintained also in the picture search mode.

(b) Capstan servo's reference signal

Record mode

The capstan servo phase servo during the record mode selects the same reference signal as that of playback mode drum servo. The clock signal generated from the color subcarrier (fsc) signal is fed to the REF counter that is reset by the internal ROM data, and the reference signal is generated.

Since the capstan servo controls the record-editing, picture continuity at the transient of editings are phase controlled by the record mode capstan phase servo. Therefore, the REF counter is reset by the C-FG signal for editing mode phase control. The REF counters for the drum servo circuit and for the capstan servo circuit are independent each other.

Playback mode

The playback mode capstan servo uses the same reference signal as that of playback mode drum servo but it is further delayed by the REC-CTL circuit and again delayed by the tracking delay circuit, and is then supplied to the playback mode capstan servo circuit as the reference signal.

(Conventional circuit selects the CTL signal to be delayed by the tracking delay circuit which is then used for capstan servo phase control.)

IC4001 REFERENCE SIGNAL GENERATION BLOCK

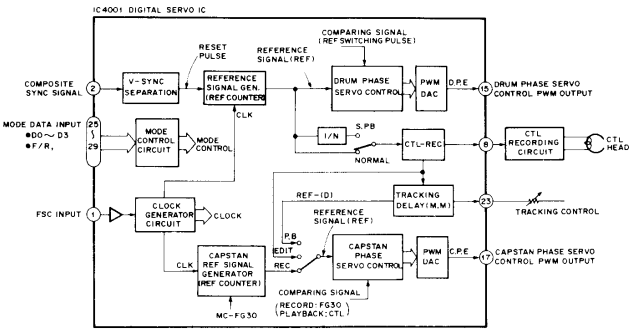


Fig. 3-4

REFERENCE SIGNAL GENERATION TIMING

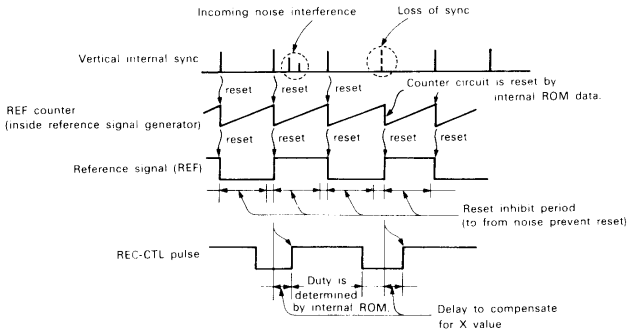


Fig. 3-5

(3) D-PG (DRUM PG) SIGNAL PROCESSING CIRCUIT (Various Switching Signals are Generated. See Fig. 3-6)

The drum PG pulse is generated in correspondence to the rotating video head phase. By receiving the D-PG input pulse, the video head rotating phase can be servo controlled (drum phase control).

The D-PG pulse is also used for the video head switching (ch-1/ch-2) signal and audio FM head switching (AF-1/AF-2) signal.

The D-PG pulse signal processing is made in the method as shown in Fig. 3-7.

The D-PG pulse, shown as ⓐ in Fig. 3-6, is routed to an amplifier IC consisting pre-amplifier and Schmitt amplifier that converts the D-PG pulse into rectangular wave shown as ⓑ in Fig.3-7. This signal is input to the digital IC pin-12 where it is delayed by the PG-DELAY circuit that is used to compensate for the mechanical mounting error of the PG coil. Delay time of the PG DELAY circuit is determined by the ⓒ and ⓓ shown in Fig. 3-7, which determine the video head CH-1/CH-2 switching position adjustment. The delayed D-PG signal ⓔ generates the RF switching pulse shown as ⓕ. The RF switching pulse is used for comparator signal of the drum phase servo, is used also for head select signal in the video head pre-amplifier and is used also for the system control timing signal.

D-PG PROCESS CIRCUIT

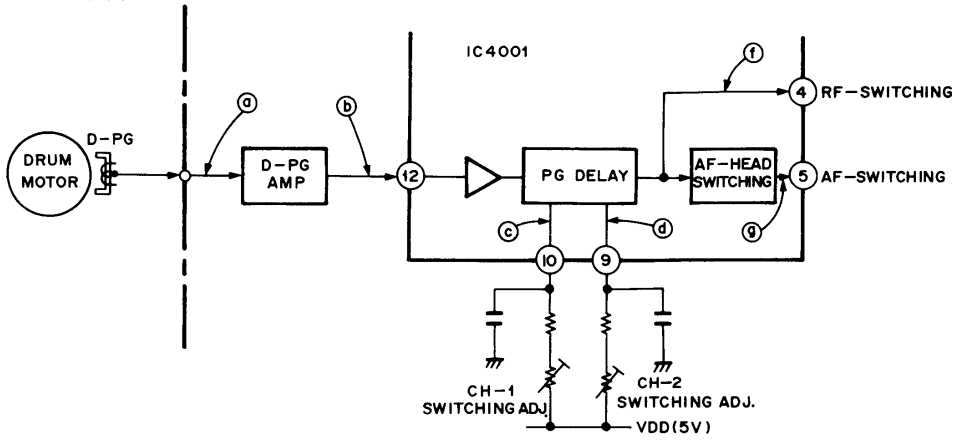
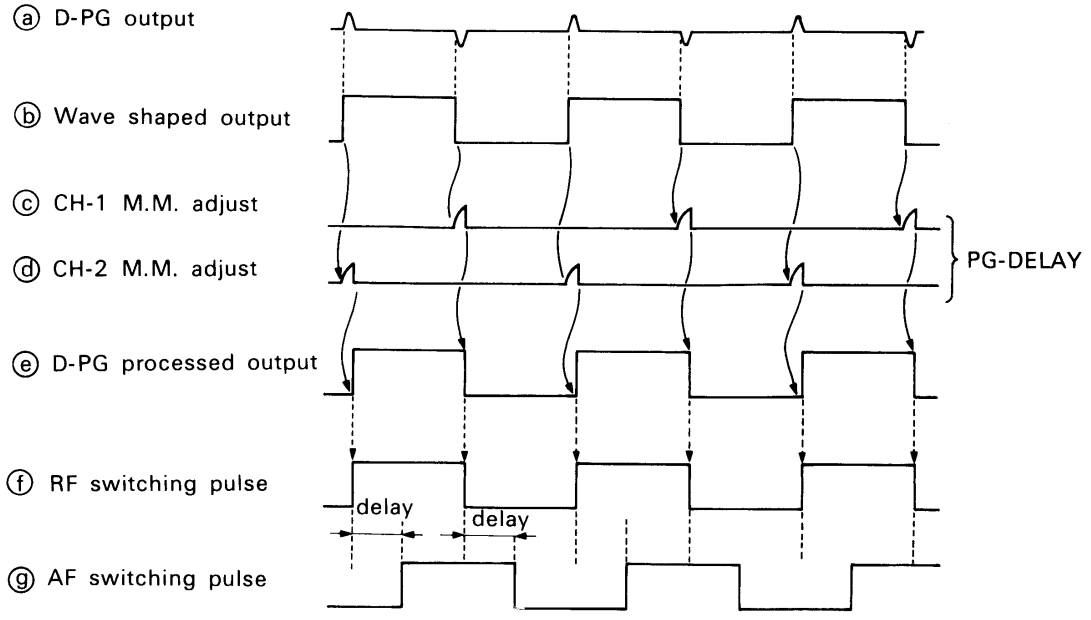


Fig. 3-6

D-PG (DRUM-PG) PROCESSING TIMING CHART



(Delay in accordance with AF head mounting angle)

Fig. 3-7

(4) DUMMY V_D SIGNAL (V-LOCK PULSE) GENERATOR CIRCUIT (V_D-GENERATOR)

The vertical sync jitter in the special playback mode can be prevented by inserting a stable dummy vertical sync signal. The dummy V_D signal generator circuit block is shown in Fig. 3-8.

The dummy V_D signal is generated from the RF switching pulse shown as ⓐ in Fig. 3-9. Though the CH-1 circuit delay is of fixed value as shown in ⓒ, the CH-2 circuit delay is made variable by the CR time constant connected to DL-2 terminal, in order to fine-adjust the vertical sync jitter compensation. The width of the dummy V_D pulse is set by a built-in counter. The dummy V_D signal that is output only during special playback mode from the V_D-OUT terminal is inserted into the playback video signal in the video circuit.

DUMMY V_D SIGNAL GENERATOR CIRCUIT BLOCK (INSIDE DIGITAL SERVO IC)

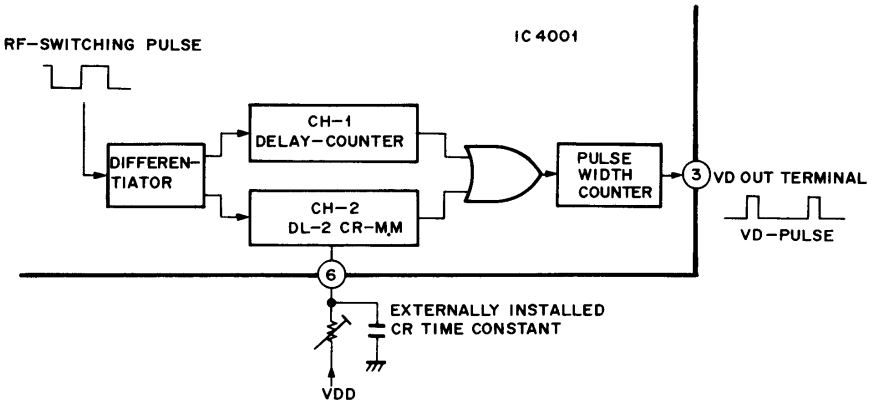


Fig. 3-8

DUMMY V_D SIGNAL GENERATION TIMING

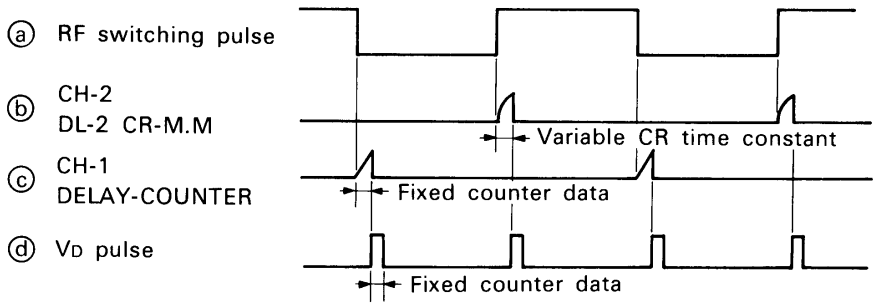


Fig. 3-9

3-3. IC4002 (LA7116), SERVO AMPLIFIER IC (Fig. 3-10)

The main servo circuit consists of this IC (LA7116) and IC4001 (LC7412). The afore-mentioned digital servo IC IC4001 (LA7412) includes all the servo control function so that this IC has the following amplifier circuits.

- Drum servo speed/phase error voltages' mixing amplifier (op. amp)
- Capstan servo speed/phase error voltages' mixing amplifier (op. amp)
- Drum FG pulse amplifier: pre-amplifier (op.amp) and wave shaper (Schmitt)
- Drum PG pulse amplifier: pre-amplifier (op.amp) and wave shaper (Schmitt)
- Capstan FG amplifier: pre-amplifier (op.amp) and wave shaper (Schmitt)
- Playback CTL amplifier: pre-amplifier (op.amp) and wave shaper (Schmitt)

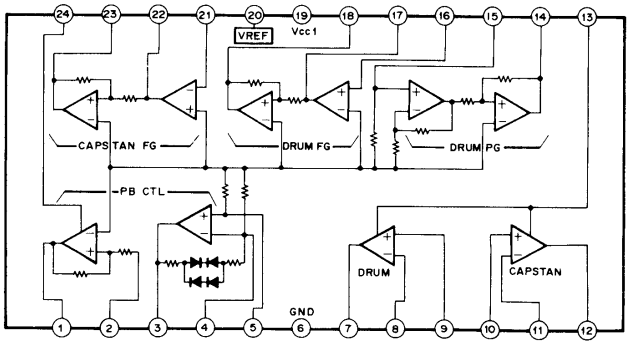


Fig. 3-10

3-4. DRUM SERVO CONTROL CIRCUIT (Fig. 3-11)

Fundamental block diagram of the drum servo control circuit is shown in Fig. 3-11. The reference signals and comparing signals required for the drum servo control are shown in table 3-2.

(1) DRUM SPEED SERVO CONTROL

As shown in table 3-2, the drum speed servo control relies upon the FG (D-FG: drum-frequency-generator) signal that is indicating rotating speed of head drum. The D-FG signal is first shaped into a chain of rectangular pulse by pre-amplifier and Schmitt amplifier, and then input to the speed control circuit of the digital servo IC. Inside the IC's speed control circuit, the D-FG's frequency is measured by the reference clock counter so that the counted value is compared with internal ROM data corresponding to target frequency. The comparison output is the servo error signal to be supplied to drum motor. The servo error signal is routed PWM-DAC circuit so that it is output as the PWM signal to be supplied from D.S.E. terminal. The PWM output signal is converted into dc voltage by the L.P.F. made of capacitor and resistor. The dc output voltage is supplied to the differential amplifier's (+) terminal that is the mixing amplifier of the speed error signal and phase error signal. The relation between L.P.F. output dc voltage and the D-FG frequency (i.e. head drum rotating frequency is shown in Fig. 1-12.

In the drum speed servo control, the D-FG input frequency is servo controlled to become same frequency as the ROM's target frequency fo. When both frequencies become equal, the PWM output signal of the DSE terminal has duty 50%. In picture search playback mode, different ROM data are taken out from ROM to control the D-FG frequency corresponding to search speed so that the horizontal frequency of playback video output is compensated. In all modes other than playback mode and record mode, the DSE terminal is set LOW to stop the drum rotation.

(2) DRUM PHASE SERVO CONTROL

The drum phase servo uses the reference signal and the comparing signal, as shown in table 3-11. The PG (D-PG) signal is used as the comparing signal, that is indicating drum motor's rotating phase. The reference signal in the record mode is the reference signal that is pre-set to the incoming video signal's vertical sync. The reference signal in the playback mode is the reference signal that is pre-set to the internal ROM data.

The comparing signal i.e. D-PG signal is first shaped into a chain of rectangular pulse by the pre-amplifier and Schmitt amplifier and is input to the digital servo IC's RF-switching pulse generator circuit. The RF-switching pulse output and the afore-mentioned reference signal are phase compared by the phase comparator circuit.

The phase comparator circuit measures the time difference between the RF switching pulse and the reference signal. The measured time difference output is compared with the internal ROM data that is corresponding to the target time difference. This comparator output is the servo error output that is routed to the PWM-DAC circuit to output the servo error signal in the PWM signal from the D.P.E. terminal. The PWM output is converted to dc voltage by L.P.F. by capacitor and resistor network and is then applied to the differential amplifier's (−) terminal that functions as the mixing amplifier of phase servo output and speed servo output dc voltages.

The relation between the L.P.F. output dc voltage and the reference/comparing signals time difference is shown by the inclined dotted line in Fig. 3-12.

The voltage control characteristics of the drum speed servo/phase servo are in opposite curves as shown in Fig. 3-12, due to operating characteristics of the differential amplifier which amplifies the servo error voltage and feeds drum motor.

In the drum phase servo control, the time difference between the reference signal and the comparing signal is designed to be equal to the inter ROM target time difference (t0). When both becomes of equal value, the PWM output waveform at the D.P.E. terminal will have duty 50%. In all modes other than playback mode and record mode, the PWM output waveform at D.P.E. has duty 50% fixed so that the drum phase servo control loop is cut off.

DRUM SERVO BLOCK

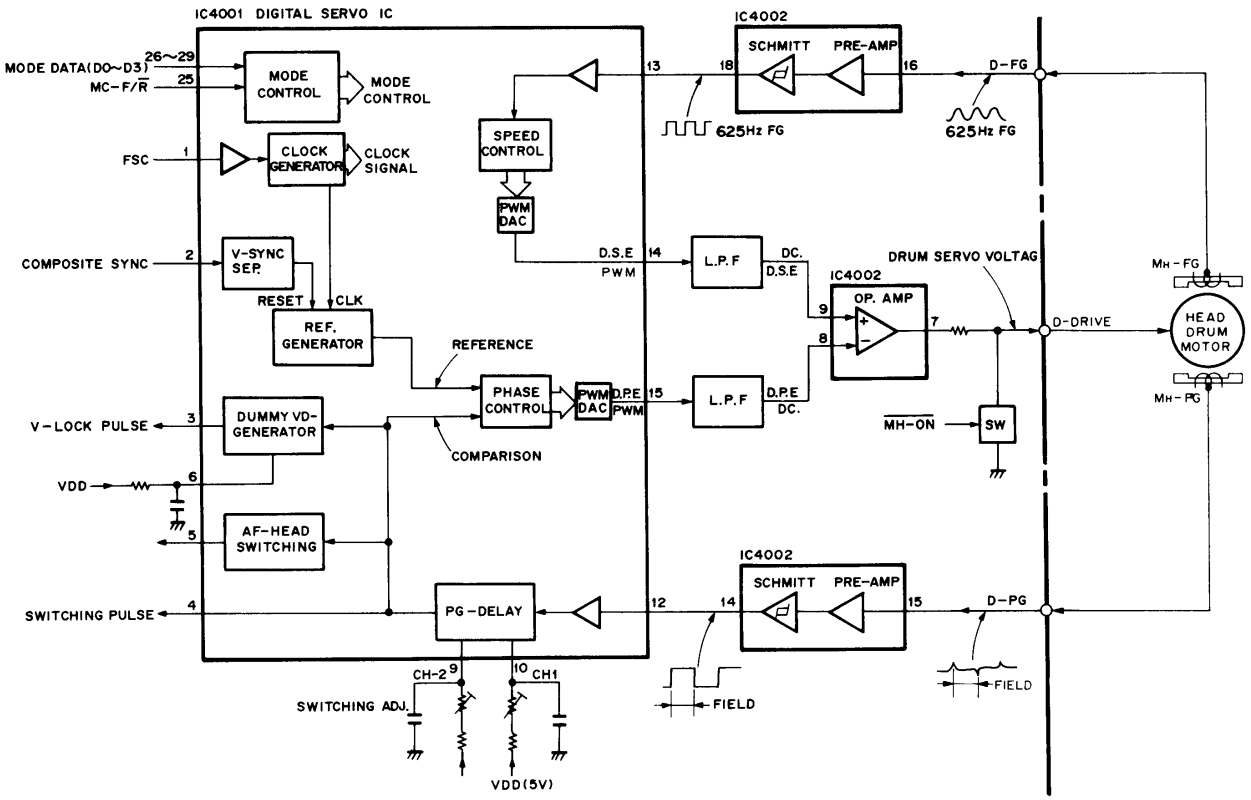


Fig. 3-11.

	Reference signal		Comparing signal
	Record	Playback	
Speed servo control	FG signal produced by the drum rotation		
Phase servo control	Reference signal that is reset by vertical sync	Reference signal that is reset by internal ROM data	RF switching pulse produced from the drum PG signal

Table 3-2.

SPEED (DSE)/PHASE (D.P.E) CONTROL VOLTAGE

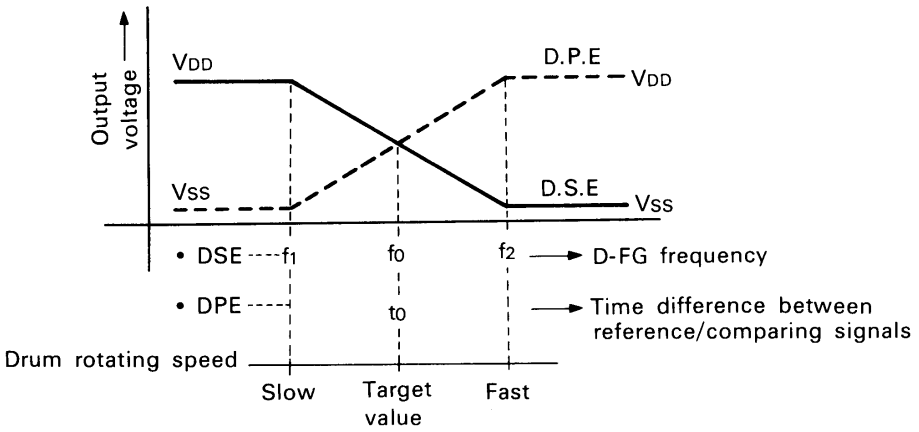


Fig. 3-12

3-5. CAPSTAN MOTOR SERVO CONTROL CIRCUIT (Fig. 3-13)

Fundamental block diagram of the capstan motor servo control system is shown in Fig. 3-13.
The capstan servo circuit and the drum servo circuit are all the same except for reference signal and comparing signal. The forward/reverse rotation direction command to the capstan motor is input from system control circuit. The rotation direction signal is the Mc-F/$\overline{R}$ signal is directly input to the motor drive circuit.

(1) CAPSTAN SPEED SERVO CONTROL

The capstan speed servo uses the FG (C-FG) signal that indicates the capstan motor rotation. The C-FG signal is shaped into rectangular wave by the preamplifier and Schmitt amplifier. The C-FG signal is input to the frequency divier circuit for digital servo special playback system.

The frequency division is performed in accordance with the selected tape speed in the picture search mode. In other word, the frequency division ratio of the C-FG signal is inversely proportional to the tape speed selected in the picture search mode. By use of this frequency division circuit all the same frequency of the C-FG signal is input regardless of normal playback/record/special playback (picture search) modes. In the capstan speed servo control circuit, the C-FG signal frequency is counted by the reference clock in the same manner as in the drum speed servo control system. The counted output and the internal ROM target data are compared.

The servo error signal is output in the form of PWM signal through PWM-DAC from C.S.E. terminal. The PWM waveform signal is converted to dc voltage by L.P.F. using capacitor and resistor, and is then routed to a differential amplifier that is mixing the speed servo error and phase servo error signals. The speed servo error signal is fed to its (+) terminal. The relationship between the servo error dc voltage after L.P.F. and the C-FG (capstan FG signal representing the capstan rotation speed) is shown in Fig. 3-14.

(2) CAPSTAN PHASE SERVO CONTROL

The capstan phase servo system, as shown in table 3-3, selects the reference signal and comparing signal according to the mode control control signal that is the mode of VCR. This servo features that the tracking control is done by delaying the reference signal in playback mode. The reference signal is delayed by the REC-CTL delay circuit and the tracking delay circuit. It also features that the reference signal is frequency divided by 1/n divider circuit that corresponds to the slow playback tape speed (n), in the models that has constant (continuous) slow playback function.
The comparing signal is selected in the record mode and playback mode separately as shown below.

Record mode

The C-FG (capstan FG) signal that is used in the capstan speed servo is also used after it is frequency divided by the internal divider (FG 25 divider) until it has same frequency as that of reference signal.

Playback mode

The playback mode selects the control (CTL) signal output that is obtained by picking up the control track signal which is recorded during the recording mode. Since this CTL signal is indicating the capstan motor rotation data, it is used as the comparing signal in the playback mode.
In the case of special playback such as picture search, the playback CTL signal to be used as comparing signal, is frequency divided by the divider (SP divider) in reverse proportional to the ratio of selected tape speed, and is then used as comparing signal. In case of reverse direction playback, the negative going edge is triggered by the F/R circuit to compensate for the tracking phase difference.

The phase servo circuit measures the time difference between the afore-mentioned reference signal and the comparing signal. The measured output is agained compared with the internally ROM data of the target time difference. This comparison output is the servo error output signal that is output from the C.P.E. terminal in the form of PWM signal. This control system and the method of conversion from PWM signal to dc voltage are exactly same is those of the drum phase servo control circuit. The characteristics of servo control voltage change in the speed servo and the phase servo have opposite inclination each other, as shown in Fig. 3-14.

CAPSTAN SERVO BLOCK

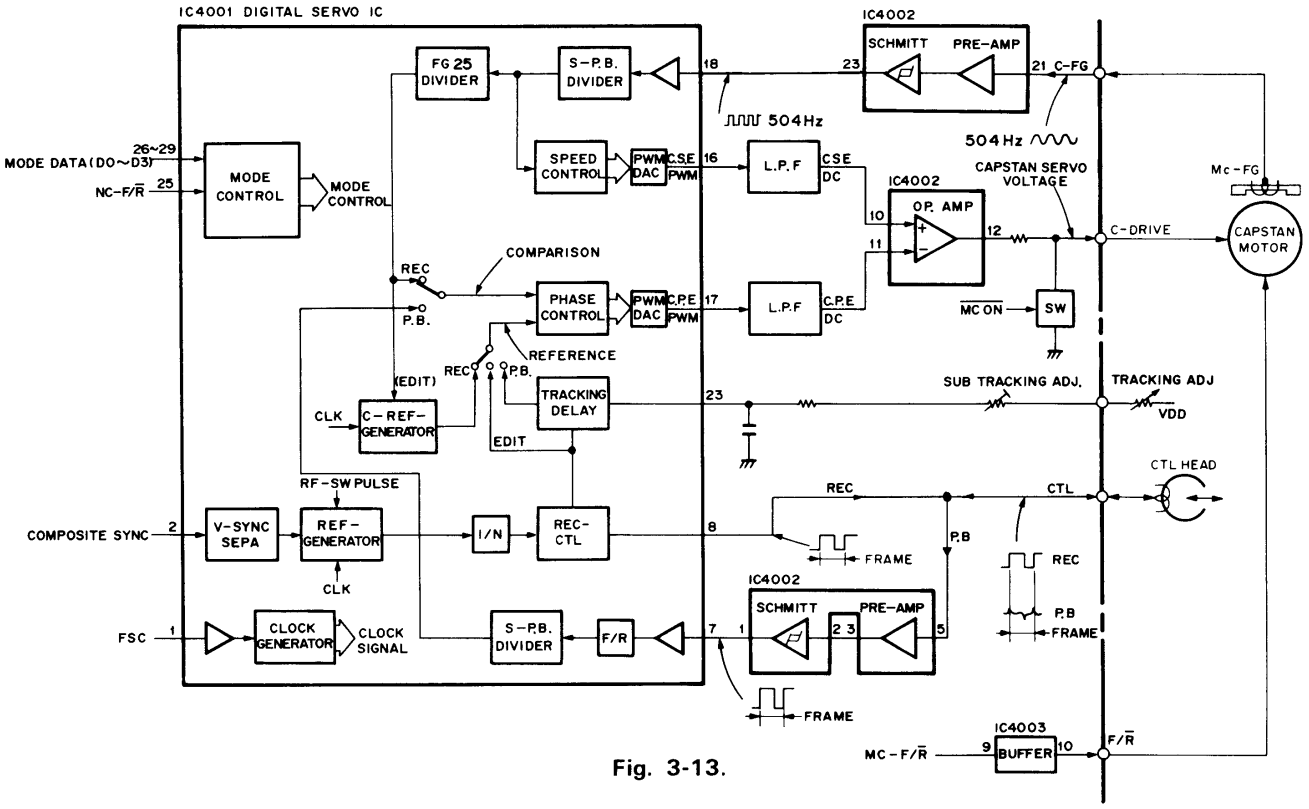


Fig. 3-13.

CAPSTAN PHASE SERVO CONTROL SIGNAL

Mode / Control signal	RECORD	PLAYBACK
Reference signal	Reference signal mode by resetting with internal ROM data	Reference signal mode by resetting with internal ROM data is delayed by tracking delay. Ref. signal is thus made
Comparing signal	The C-FG signal is frequency divided until same frequency as the reference signal	Playback CTL signal

Table 3-3.

SPEED (C.S.E)/PHASE (C.P.E) CONTROL VOLTAGE

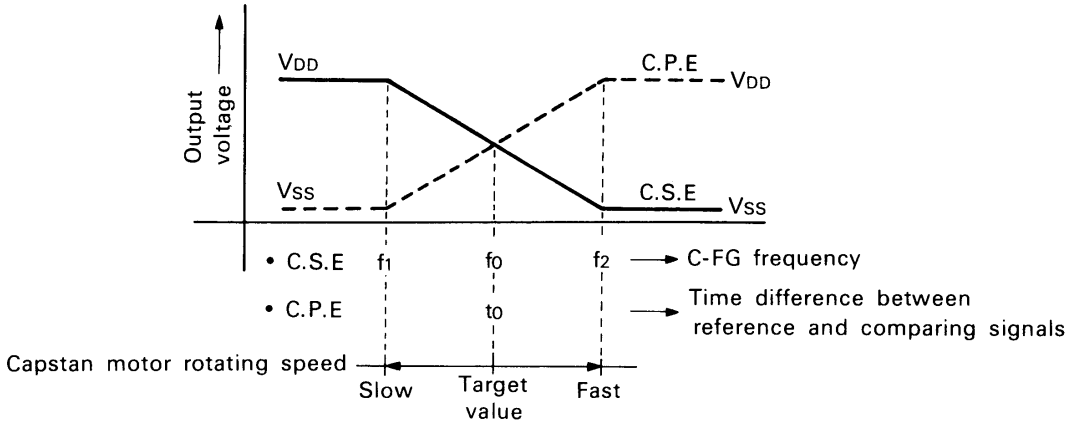


Fig. 3-14

4. SYSTEM CONTROL CIRCUIT

4-1. OUTLINE

The system control circuit consists mainly of IC3001 (SYSTEM CONTROL MPU) as shown in Fig. 4-1 block diagram.

Features of this model (comparison with conventional model VHR2100 etc.)

- The front loading operation is driven by the capstan motor, not using loading motor any more.
- The tape top/end sensor circuit is housed inside IC3001 reducing the external circuit.

4-2. IC3001 INPUT/OUTPUT TABLE

Signal processing of the system control circuit is mostly done by the IC3001. The I/O table for IC3001 is shown in table 4-1.

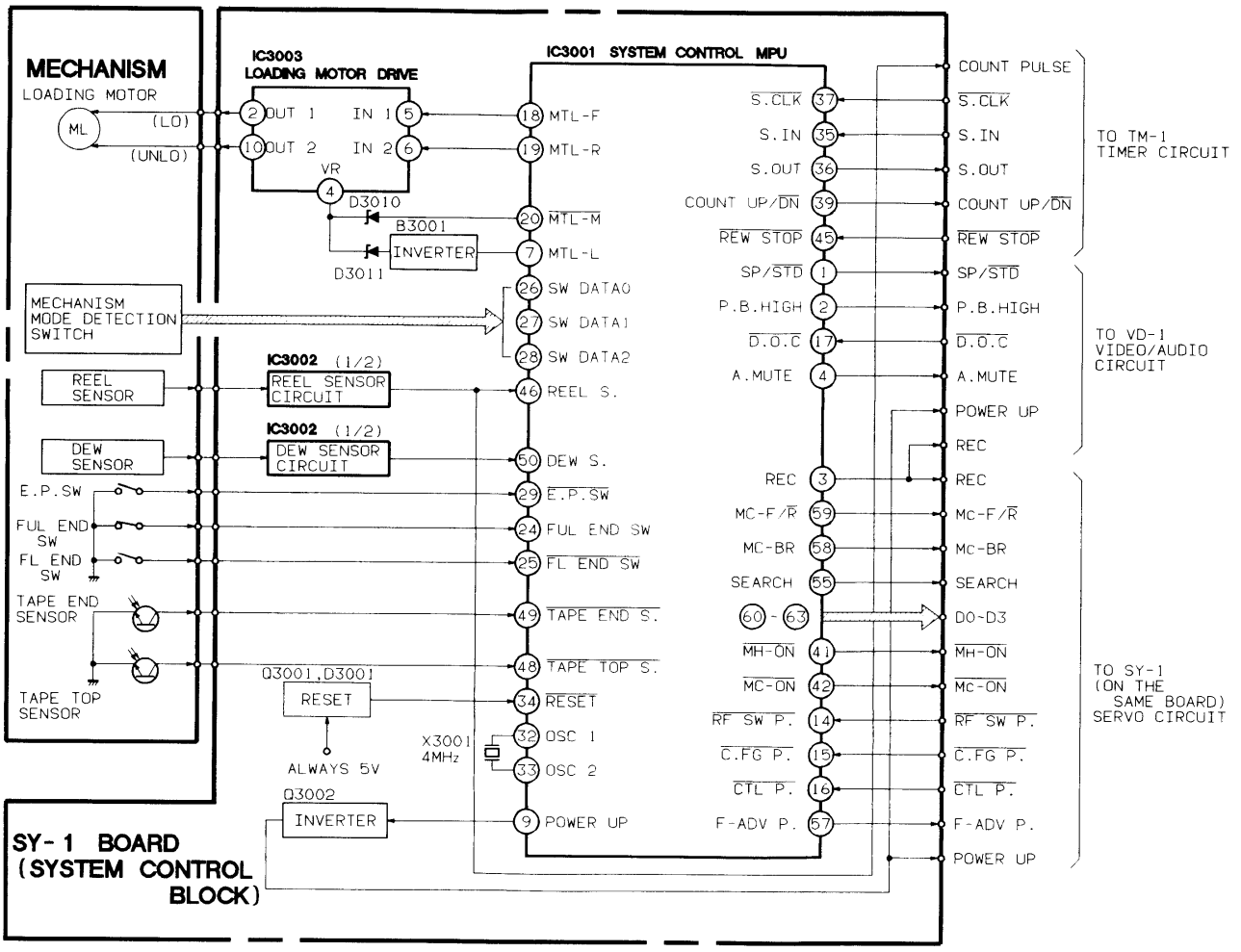


Fig. 4-1

SYSTEM CONTROL MPU (IC3001: LC6568H3350)

PIN NO.	PORT NAME	INPUT/OUTPUT NAME	I/O	FUNCTION
1	PN0	SP/$\overline{STD}$	O	Output during special playback mode. (F/R-SEARCH, STILL)
2	PN1	P.B. HIGH	O	Signal mainly used for E-E picture/playback picture switching.
3	PN2	REC	O	Output during record mode.
4	PN3	AUDIO MUTE	O	Signal to inhibit audio signal; mainly output during special playback mode.
5	PO0	AUDIO REC MUTE	O	Not used.
6	PO1	AUDIO BIAS CTL	O	Not used.
7	PO2	MTL-L	O	Signal to indicate tape loading motor (MTL) low speed rotation.
8	PO3	STILL + SLOW2	O	Not used.
9	PP0	POWER UP	O	VCR power supply ON/STAND BY control signal.
10	PA0	OPTION 0	I	Use/inhibit indication terminal of F-ADV, 1/5 SLOW and 1/10 SLOW function programmed within MPU; inhibited when LOW input.
11	PA1	OPTION 1	I	
12	PA2	OPTION 2	I	X2 speed playback function inhibited when this terminal is LOW.
13	PA3	DIRECT P.B. INH.	I	Use/inhibit indication terminal of DIRECT PLAY function programmed within MPU; inhibited when LOW input.
14	INT0	$\overline{RF\ SW\ PULSE}$	I	Head motor (MH) rotation detection signal.
15	INT1	$\overline{C.\ FG\ PULSE}$	I	Capstan motor (MC) rotation detection signal; used for MC-BRAKE (Pin 58) pulse width control.
16	INT2	$\overline{CTL\ PULSE}$	I	Control (CTL) pulse input.
17	INT3	$\overline{D.\ O.\ C.}$	I	Drop-out signal input.
18	PC0	MTL-F	O	Signal to indicate tape loading motor (MTL) rotation — loading.
19	PC1	MTL-R	O	Signal to indicate tape loading motor (MTL) rotation — unloading.
20	PC2	$\overline{MTL\text{-}M}$	O	Signal to indicate tape loading motor (MTL) middle speed rotation.
21	PC3	ANT/$\overline{VIDEO}$	O	Not used.
22	PD0	AV CONTROL	I	Not used.
23	PD1	PAUSE SW	I	Not used.
24	PD2	FUL END SW	I	Front-unloading-end switch input.
25	PD3	$\overline{FL\ END\ SW}$	I	Front-loading-end switch input.
26	PE0	SW DATA 0	I	Mechanism mode detection switch input. Input to pins 26, 27 and 28 by 3-bit code in table at right.
27	PE1	SW DATA 1	I	
28	PE2	SW DATA 2	I	
29	PE3	$\overline{E.\ P.\ SW}$	I	Accidental-erase-prevention switch input.
30	TEST			Normally ground.
31	Vss			MPU ground terminal.
32	OSC1			System clock (4 MHz).
33	OSC2			
34	$\overline{RES}$	$\overline{RESET}$	I	MPU initial reset terminal.
35	S. IN	S. IN	I	IR remote-control operation signals and operation signals related to timer sent from timer MPU as 8-bit code.
36	S. OUT	S. OUT	O	Tape speed, cassette in, dew indication signals and timer operation designation signals are sent to timer MPU as 8-bit code.
37	$\overline{S.\ CLK}$	$\overline{S.\ CLK}$	I	Transmission/reception timing signal for serial transfer; sent from timer MPU.

MODE POSITION \ SW INPUT	SW DATA 2	SW DATA 1	SW DATA 0
① EJECT	0	0	1
Mode shift intermediate position.	0	0	0
② FF, REW	0	1	0
Mode shift intermediate position.	0	0	0
③ STOP	0	1	1
Mode shift intermediate position.	0	0	0
④ PLAY, REC, F-SEARCH	1	0	0
Mode shift intermediate position.	0	0	0
⑤ STILL	1	0	1
Mode shift intermediate position.	0	0	0
⑥ R-SEARCH	1	1	0

PIN NO.	PORT NAME	INPUT/OUTPUT NAME	I/O	FUNCTION
38	PH0	TAPE SPEED SW2	O	Not used.
52	PK0	TAPE SPEED SW1	O	
39	PG0	COUNT UP/$\overline{DOWN}$	O	Signal to indicate tape counter — addition/subtraction.
40	PG1	STILL + SLOW1	O	Not used.
41	PG2	$\overline{MH\text{-}ON}$	O	Signal to indicate head motor (MH) rotation or stop.
42	PG3	$\overline{MC\text{-}ON}$	O	Signal to indicate capstan motor (MC) rotation or stop.
43	PI0	$\overline{SP}$/EP	I	Not used.
44	PI1	LP	I	
45	PI2	$\overline{REW\ STOP}$	I	Counter memory stop signal (Output by tape counter "0000"); accepted only during rewind.
46	PI3	REEL SENSOR	I	Detects tape take-up reel pulse input.
47	REF B	REF. TAPE SENSOR	I	Tape top/end sensor reference voltage input.
48	CMP B1	$\overline{TAPE\ TOP\ SENSOR}$	I	Sensor signal detection of pressure of tape cassette and both ends of tape (table at right).
49	CMP B2	$\overline{TAPE\ END\ SENSOR}$	I	
50	CMP B3	DEW SENSOR	I	Mechanism moisture condensation (dew) detection sensor signal.
51	VP			Normally ground.
53	PK1	X2S	O	Not used.
54	PK2	HI SPEED SEARCH	O	Not used.
55	PK3	SEARCH	O	Output during F/R search mode.
56	PL0	CTL INHIBIT	O	Not used.
57	PL1	F-ADV. PULSE	O	High pulse is output at fixed cycles the F-ADV. mode.
58	PL2	MC-BRAKE	O	Signal to indicate capstan motor (MC) brake.
59	PL3	MC-F/$\overline{R}$	O	Signal to indicate capstan motor (MC) — CW/CCW rotation.
60	PM0	D0	O	Output to servo circuit by 4-bit code at right as mode control signal.
61	PM1	D1	O	
62	PM2	D2	O	
63	PM3	D3	O	
64	VDD			Power supply terminal.

TAPE TOP SENSOR	TAPE END SENSOR	TAPE ENDS DETECTION	CASSETTE IN/OUT
OFF	OFF	X	IN
OFF	ON	Beginning of tape	IN
ON	OFF	End of tape	IN
ON	ON	X	OUT

OPERATION MODE	*	D3	D2	D1	D0
STOP	⓪	0	0	0	0
FL, FUL	①	0	0	0	1
TL, TUL	②	0	0	1	0
FF, REW	③	0	0	1	1
MODE SHIFT (PLAY)	④	0	1	0	0
MODE SHIFT (E-E)	⑤	0	1	0	1
MODE SHIFT	⑥	0	1	1	0
REC	⑦	0	1	1	1
PAUSE	⑧	1	0	0	0
MODE SHIFT (PLAY)	⑨	1	0	0	1
PLAY	Ⓐ	1	0	1	0
X2 SPEED PLAY	Ⓑ	1	0	1	1
F/R SEARCH	Ⓒ	1	1	0	0
HI SPEED SEARCH	Ⓓ	1	1	0	1
SLOW 1	Ⓔ	1	1	1	0
SLOW 2	Ⓕ	1	1	1	1

* Indicates hexadecimal substitution.

Table 4-1

5. TIMER AND CHANNEL PRESET CIRCUIT

5-1. OUTLINE

As shown in Fig. 5-1 Block diagram, this circuit is configured around IC7401 (Timer and Channel Preset MPU).
This model has the same fundamental circuit configuration as previous model VHR-2100, etc. Model VHR-3100 EX/G is equipped to handle VPS. (The VPS decoder SVP-10 is fundamentally a common circuit with the circuit for the VHR-2100.)

5-2. IC7401 INPUT/OUTPUT TABLE

Almost all processing for the Timer and Channel Preset Circuits is performed by IC7401. The I/O table for IC7401 is shown in Table 5-1.

TIMER AND CHANNEL PRESET MPU (IC7401:M50754-686SP)

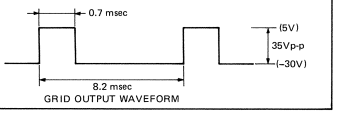
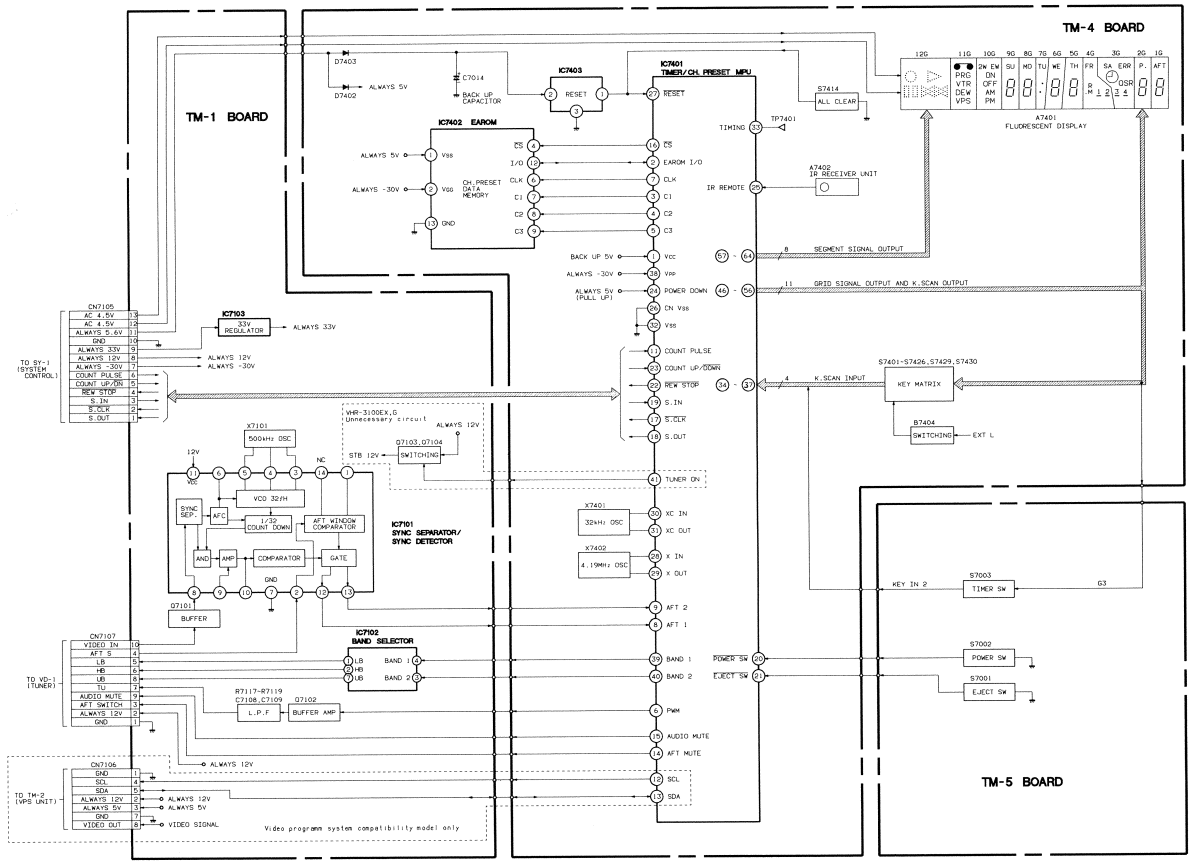
PIN No.	PORT NAME	INPUT/OUTPUT NAME	I/O	FUNCTION
1	VCC	BACK UP 5V		Power supply (BACK UP 5V) terminal.
2	P65	EAROM I/O	I/O	Channel preset data input/output terminal.
3	P64	EAROM C1	O	Signal to indicate mode control (read, write, address, data).
4	P63	EAROM C2	O	
5	P62	EAROM C3	O	
6	P61	PWM	O	Tuning data (14-bit) output terminal.
7	P60/T	EAROM CLK	O	Transmission/reception timing signal for serial transfer; sent to EAROM (IC7402).
8	P27	AFT1	I	AFT recognition signal (2-bit) input from SYNC SEP./SYNC DET. IC (IC7101).
9	P26	AFT2	I	
10	P25	SECAM L/B/G	I	Not used.
11	P24	COUNT PULSE	I	Tape count pulse input.
12	P23	SCL	O	Transmission/reception timing signal for serial transfer; sent to VPS unit.
13	P22	SDA	I/O	VPS data input/output terminal.
14	P21	AFT MUTE	O	Signal to defeat AFT signal.
15	P20	AUDIO MUTE	O	Signal to inhibit audio signal.
16	P37/$\overline{SRDY}$	$\overline{EAROM\ CS}$	O	EAROM (IC7402) chip select terminal.
17	P36/CLK	$\overline{S.CLK}$	O	Transmission/reception timing signal for serial transfer; sent to system-control MPU.
18	P35/SOUT	S.OUT	O	IR remote-control operation signals and operation signals related to system-control sent to system-control MPU.
19	P34/SIN	S.IN	I	Cassette in, dew indication signals and timer operation designation signals are sent from system-control MPU.
20	P33	$\overline{POWER\ SW}$	I	Power switch input.
21	P32	$\overline{EJECT\ SW}$	I	Eject switch input.
22	P31	$\overline{REW\ STOP}$	O	Counter memory stop signal (output by tape counter "0000").
23	P30	COUNTUP/$\overline{DOWN}$	I	Signal to indicate tape counter – addition/subtraction.
24	P53/INT1	POWER DOWN	I	Power failure detection terminal.
25	P52/INT2	IR REMOTE	I	IR remote-control operation signals input.
26	CN Vss			Normally ground.
27	$\overline{RESET}$	$\overline{RESET}$	I	MPU initial reset terminal.
28	X IN			System clock (4.19 MHz)
29	X OUT			
30	XC IN			Power failure clock (32 kHz)
31	XC OUT			
32	Vss			MPU ground terminal.
33	ϕ	TIMING		Test terminal.
34	P57	K.SCAN IN 4	I	Operation button keyscan signals input.
35	P56	K.SCAN IN 3	I	
36	P55	K.SCAN IN 2	I	
37	P54	K.SCAN IN 1	I	
38	VP	ALWAYS-30V		Power supply (ALWAYS-30V) terminal.
39	P51	BAND1	O	Switch data (2-bit) output designate band position.
40	P50	BAND2	O	
41	P17	TUNER ON	O	Tuner ON/OFF control signal.
42	P16	SECAM L		Not used.
43	P15			Not used.
44	P14			Not used.
45	P13			Not used.
46	P12	GRID 11	O	The fluorescent display tube is illuminated by the dynamic illumination method. * Grid-output signals The respective signals are always output at a cycle of about 8.2 msec. * Segment-output signals These signals are output at the same timing as the grid, and are, output only when necessary. * Keyscan-output signals These signals are output at the same timing as the grid, and are, output key matrix circuitry.  GRID OUTPUT WAVEFORM
47	P11	GRID 10	O	
48	P10	GRID 9/K.SCAN OUT	O	
49	P07	GRID 8/K.SCAN OUT	O	
50	P06	GRID 7/K.SCAN OUT	O	
51	P05	GRID 6/K.SCAN OUT	O	
52	P04	GRID 5/K.SCAN OUT	O	
53	P03	GRID 4/K.SCAN OUT	O	
54	P02	GRID 3/K.SCAN OUT	O	
55	P01	GRID 2/K.SCAN OUT	O	
56	P00	GRID 1/K.SCAN OUT	O	
57	P47	SEGMENT h	O	
58	P46	SEGMENT g	O	
59	P45	SEGMENT f	O	
60	P44	SEGMENT e	O	
61	P43	SEGMENT d	O	
62	P42	SEGMENT c	O	
63	P41	SEGMENT b	O	
64	P40	SEGMENT a	O	

Table 5-1


TM-4 BOARD
TM-1 BOARD
TM-5 BOARD
IC7401
TIMER/CH. PRESET MPU
IC7403
IC7402 EAROM
A7401
FLUORESCENT DISPLAY
A7402
IR RECEIVER UNIT
S7414
ALL CLEAR
TP7401
TIMING
IR REMOTE
SEGMENT SIGNAL OUTPUT
GRID SIGNAL OUTPUT AND K.SCAN OUTPUT
K.SCAN INPUT
S7401-S7426,S7429,S7430
KEY MATRIX
B7404
SWITCHING
EXT L
CN7105
TO SY-I (SYSTEM CONTROL)
IC7103
3.3V REGULATOR
ALWAYS 33V
ALWAYS 12V
ALWAYS -30V
COUNT PULSE
COUNT UP/DOWN
REW STOP
S.IN
S.CLK
S.OUT
BACK UP 5V
POWER DOWN (PULL UP)
CN Vss
Vss
Vcc
Vpp
X7101
500kHz OSC
VHR-3100EX,G Unnecessary circuit
Q7103,Q7104
SWITCHING
STB 12V
IC7101
SYNC SEPARATOR/ SYNC DETECTOR
VCO 32fH
SYNC SEP.
AFC
1/32 COUNT DOWN
AFT WINDOW COMPARATOR
AND
AMP
COMPARATOR
GATE
Q7101
BUFFER
X7401
32kHz OSC
X7402
4.19MHz OSC
TUNER ON
XC IN
XC OUT
X IN
X OUT
AFT 2
AFT 1
IC7102
BAND SELECTOR
LB
HB
UB
BAND 1
BAND 2
CN7107
TO VD-I (TUNER)
VIDEO IN
AFT S
TU
AUDIO MUTE
AFT SWITCH
R7117-R7119
C7108,C7109
Q7102
L.P.F
BUFFER AMP
PWM
AUDIO MUTE
AFT MUTE
SCL
SDA
CN7106
TO TM-2 (VPS UNIT)
VIDEO SIGNAL
Video programm system compatibility model only
S7003
TIMER SW
KEY IN 2
S7002
POWER SW
S7001
EJECT SW
POWER SW
EJECT SW

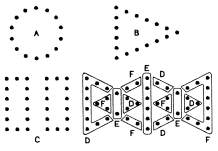
5-3. FLUORESCENT DISPLAY CIRCUIT

The lighting method of the fluorescent display is the dynamic lighting method which is the same as conventional models.
Fig. 5-2 shows the grid assignment and Table 5-2 shows the grid/segment connections.

	12G	11G	10G	9G	8G	7G	6G	5G	4G	3G	2G	1G
a	B	PRG	2W	a	a	—	a	a	M	ERR	a	a
b	—	—	ON	b	b	—	b	b	1	◷	b	b
c	E	—	AM	c	c	—	c	c	▬	4	c	c
d	—	VPS	PM	d	d	—	d	d	DP	▬	d	d
e	F	DEW	—	e	e	col	e	e	▬	▬	e	e
f	D	VTR	EW	f	f	—	f	f	R	QSR	f	f
g	C	—	OFF	g	g	—	g	g	2	3	g	g
h	A	☎	—	SU	MO	TU	WE	TH	FR	SA	P	AFT

Fig. 5-1

SEGMENT DESIGNATION



GRID ASSIGNMENT

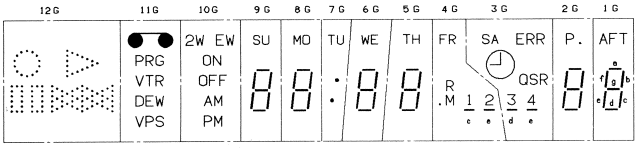


Fig. 5-2

6. TUNER, IF CIRCUIT

The tuner and IF circuits are located in sealed cases and attached to the VD-1 board.
Fig. 6-1 shows the IF circuit (VHR-3100EX/G) block diagram.

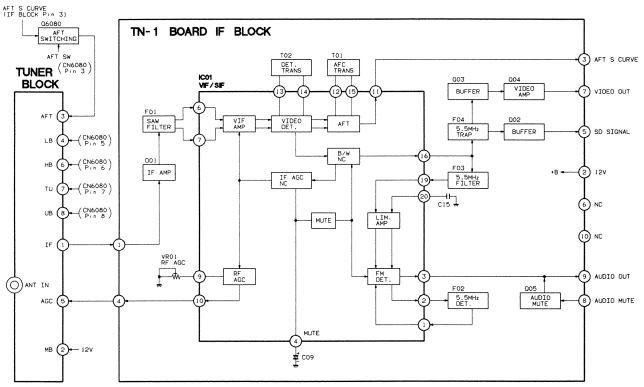


Fig. 6-1

7. POWER SUPPLY CIRCUIT

Fig. 7-1 shows the power supply circuit (VHR-3100EX/G)block diagram.

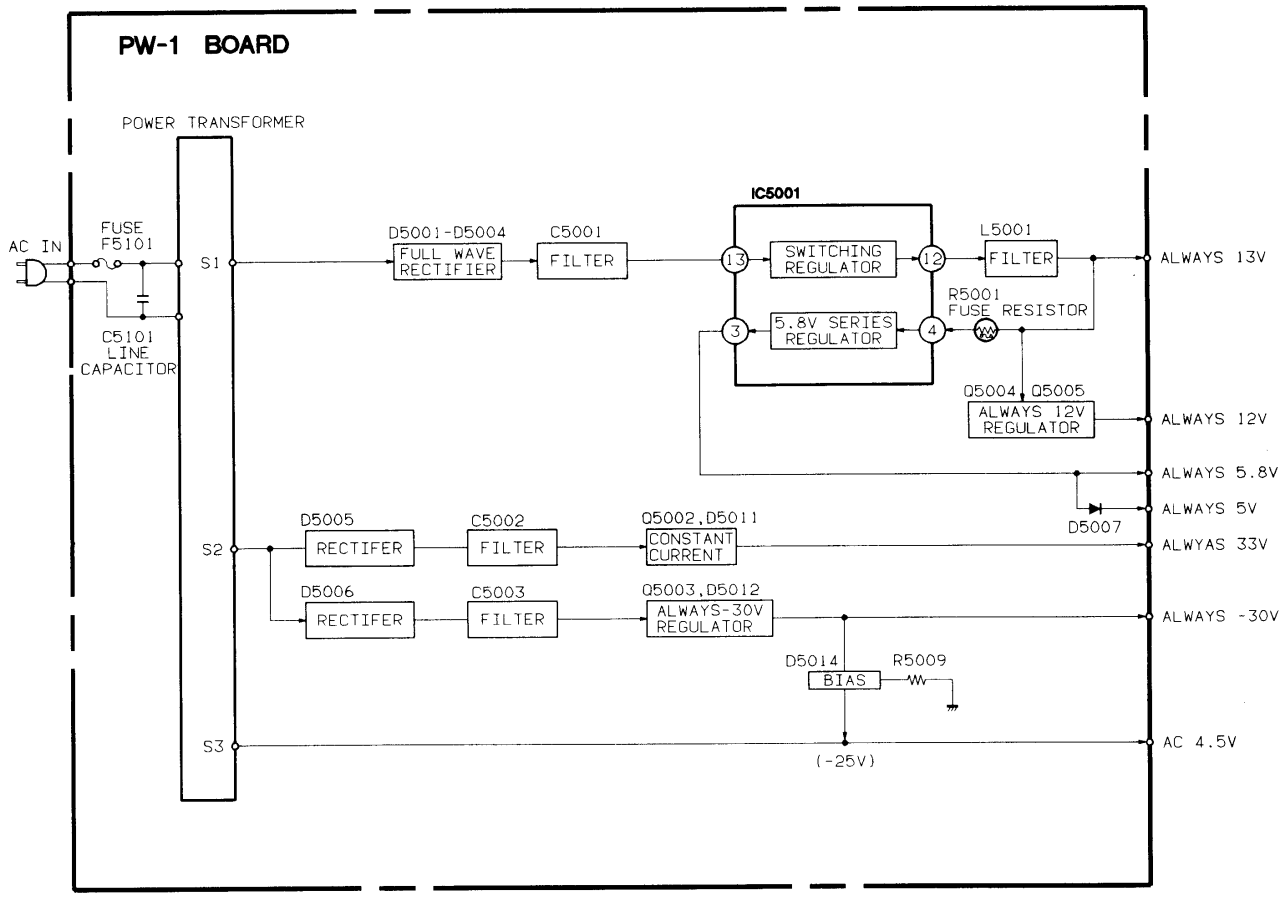


Fig. 7-1

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